IEEE 802.3af PoE PD with Integrated DC-DC Controller and 13W Power FET

Features

- Compliant to IEEE® Std. 802.3af-2003
- Supports Type 1 operation for IEEE® 802.3at-2009 and IEEE® 802.3bt-2018
- Integrated DC-DC Controller with robust 150V, 0.7Ω typ. supporting both isolated and non-isolated applications
- Low R_{DS_ON} Hot-Swap FET, 0.49Ω typ.
- Adjustable switching frequency from 100kHz to 800kHz
- Programmable DC-DC Current Limit
- Integrated Surge Protection for 15kV/8kV System level ESD Compliance
- Exceptional EMI performance
- Integrated Short-Circuit Protection
- Over temperature protection
- RoHS & Pb Free 4x4 mm, 16 lead TQFN Package
- Industrial temperature range (-40°C to +85°C)

Applications

- Pan, tilt and zoom (PTZ), security and web cameras
- Voice over IP (VoIP) phones
- Wireless LAN access points, biometric authentication
- Point-of-sale (POS) terminals, RFID terminals
- Thin clients and IoT appliances
- Fiber-to-the-home (FTTH) terminals

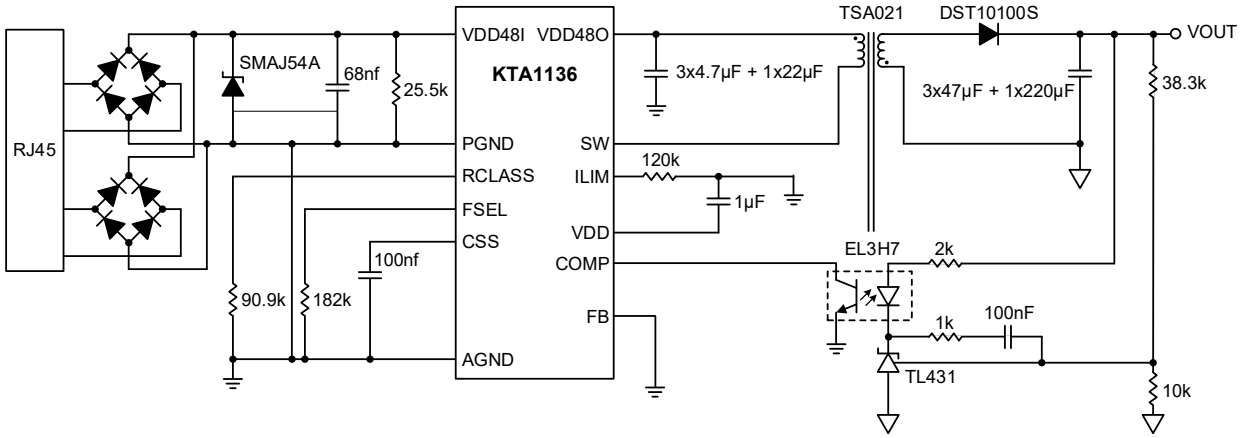
Brief Description

The KTA1136 is a single-chip, highly integrated CMOS solution for 13W Power over Ethernet (PoE) Powered Devices. Applications include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security Cameras, WiMAX Terminals, Point-of-Sales Terminals, RFID Readers, Thin Clients and Notebook computers.

The KTA1136 integrates input surge protection, a PD controller with a 100V hot-swap FET, a DC-DC controller, and a robust 150V switching power MOSFET. The KTA1136 implements all the physical layer Powered Device (PD) functionality, as required by IEEE 802.3af-2003 standards. This includes PD detection, classification, under-voltage lockout (UVLO), and Hot-Swap FET integration. The KTA1136 also supports Type 1 operation for IEEE 802.3at-2009 and IEEE 802.3bt-2018.

The KTA1136 has been architected to address both EM emission concerns and surge/over-voltage protection in PoE applications. The chip implements many design features that minimize transmission of system common-mode noise onto the Unshielded Twisted Pair (UTP). On-chip integration of surge protection provides faster response to surge events and limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY. The device is designed to provide safe, low-impedance discharge paths directly to the earth ground, resulting in superior reliability and circuit protection.

Typical Applications

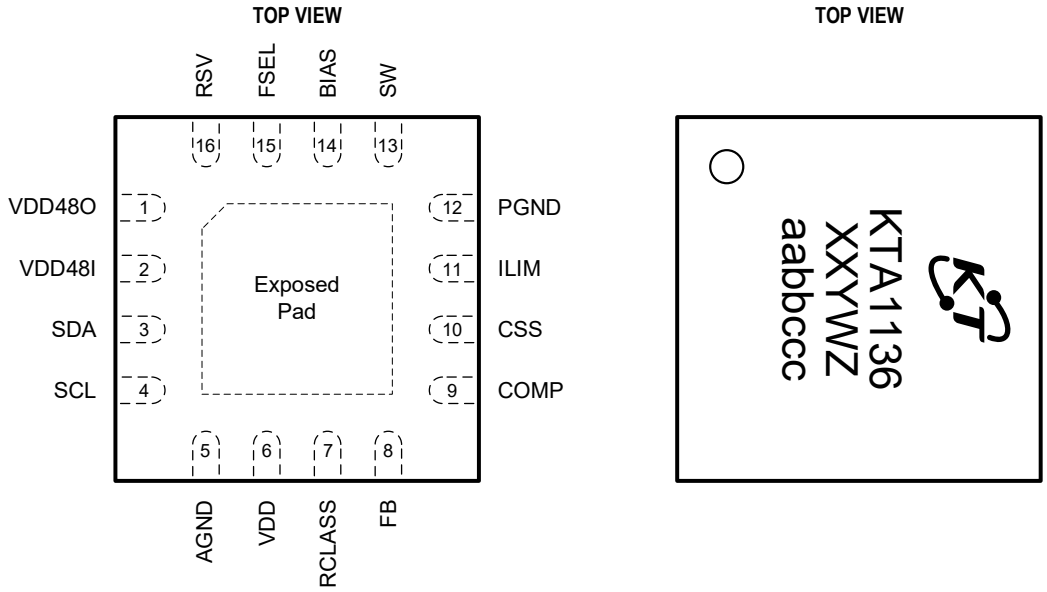


Pin Description

Pin #	I/O	Name	Function
1	P	VDD48O	Switched 48V supply output
2	P	VDD48I	48V positive bus pin, fed by the output of the external diode bridge. This bus requires the connection of a detection signature capacitor and resistor. Refer to Detection Mode section.
3	A	SDA	Internal use. Must be connected to exposed pad ground (GND)
4	A	SCL	Internal use. Must be connected to exposed pad ground (GND)
5	A	AGND	Must be connected to exposed pad ground (GND)
6	O	VDD	Internal 5 volts bus decoupling point
7	A	RCLASS	Classification resistor connection
8	A	FB	DC-DC Controller feedback point
9	A	COMP	DC-DC Controller error amplifier compensation network connection
10	A	CSS	DC-DC Controller soft-start capacitor connection point (required).
11	A	ILIM	DC-DC current limit program pin, connect a resistor between this pin and ground to set the desired current limit
12	P	PGND	Power Ground
13	P	SW	Drain connection to the internal switching power MOSFET of the DC/DC converter
14	I	BIAS	Optional input to VDD bias regulator. Powering VDD from an external supply instead of VIN can reduce power loss at high VIN. For BIAS > 7V, the VDD regulator draw current from BIAS pin. The BIAS pin voltage must not exceed 20V
15	I	FSEL	Frequency Select. This pin sets the switching frequency of the DC-DC converter.
16	A	RSV	Reserved Pin, leave it open
EP	Exposed Pad	GND	Local analog ground. This is the negative output from the external diode bridge and is not isolated from the line input.

Key: I = Input, O = Output, A = Analog Signal, P = Power, RSV = Reserved.

TQFN44-16



16-Pin 4mm x 4mm x 0.75mm
TQFN Package, 0.65mm pitch

Top Mark
XX = Device ID Code, YWZ = Date and Assembly Code
aabbccc = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VDD48I, VDD48O	High Voltage Pins[2]	100	V
SW	High Voltage Pins[2] (100µs duration,10%Duty)	150	V
BIAS	Mid Voltage Pin[2]	20	V
VDD, RCLASS, FB, COMP, CSS, ILIM, FSEL	Low Voltage Pins	6	V
T_S	Storage Temperature	165	°C
T_J	Junction Operating Temperature	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10sec)	260	°C

ESD Ratings

Symbol	Description	Conditions	Value	Units
V_{ESD_HBM}	Human Body Model (HBM)[3]	JESD22-A114	±2	kV
V_{ESD_CD}	Contact Discharge[4]	IEC 61000-4-2	±8	kV
V_{ESD_AGD}	Air-Gap Discharge[4]	IEC 61000-4-2	±15	kV

Thermal Capabilities[5]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient	30.9	°C/W
P_D	Maximum Continuous Power Dissipation at 25°C (T_J = 85°C)	1.94	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-32.4	mW/°C

Ordering Information

Part Number	Marking[6]	Operating Temperature	Package
KTA1136EUAE-TR	PQYWZaabbccc	-40°C to +85°C	TQFN44-16

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Steady state or transient conditions like system start-up and other noise conditions. Device must not be exposed to sustained over-voltage condition at this level. See section on Rectification and Protection for further details on Integrated Surge Protection.
3. Human Body Model ESD limits are all pins and specified at the chip level.
4. Air Discharge, and Contact Discharge applies to VDD48I and specified at the system level.
5. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
6. PQ = Device ID Code, YWZ = Date and Assembly Code, aabbccc = Serial Number.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.[7]	Max.	Unit
$V_{IN\ (Type\ 1\ PD)}$	Input Power supply	37.0	48.0	57.0	V
F_{SW}	Operating Switching Frequency Range	100		800	kHz
T_A	Ambient Operating Temperature Range	-40	-	+85	°C
T_{J_MAX}	Recommended Maximum Junction Operating Temperature			140	°C

Electrical Characteristics[8]

Unless otherwise noted, specifications are for T_A = -40°C to +85°C. Typical specifications are for T_A = +25°C and V_{IN} = 48V (at RJ45 Input). Typical specifications not 100% tested.

Symbol	Description	Conditions		Min	Typ	Max	Units
PD (all PD voltage limits specified at the RJ45 Interface							
I_{INRUSH}	Inrush Current Limit – Type 1 PD	For VDD48O ≤ 16V during startup, C_{IN} = 10µF		80	150	220	mA
I_{LIM}	Current Limit			500	640	800	mA
$R_{DS\text{-}ON\text{-}PD}$	Hot-Swap FET On Resistance	I_{IN} = 350mA			0.49		Ω
V_{DET_MIN}	Min Detection Signature voltage					2.7	V
V_{DET_MAX}	Max Detection Signature voltage			10.0	12.5	14.5	V
V_{CL_LOW}	Classification Lower Threshold	During Classification, the KTA1136 sinks current as defined		11.0	12.5	14.5	V
$V_{CL_LOW_HYS}$	Classification Lower Hysteresis				1.5		V
V_{CL_HIGH}	Classification Upper Threshold			20.5	22.0	25.0	V
$V_{CL_HIGH_HYS}$	Classification Higher Hysteresis				1.5		V
$V_{IN_UVLO_R}$	Input UVLO Threshold	V_{IN} Rising		35	36.5	38	V
$V_{IN_UVLO_F}$		V_{IN} Falling		30	31.5	33	V
I_{Class}	Classification Current	VDD48I = 14.5V to 20.5V; External detection resistor = 25.5K±1% Rclass Resistor = ±1% Tolerance	Class0, R_{CLASS} Pull up to VDD	0	2.5	4	mA
			Class1, R_{CLASS}=301kΩ	9	10.5	12	mA
			Class2, R_{CLASS}=147kΩ	17	18.5	20	mA
			Class3, R_{CLASS}=90.9kΩ	26	27.5	30	mA
VDD Internal Regulator							
V_{VDD}	Output Voltage	C_{VDD} = 1µF, Powering VDD from VDD48I		4.3	4.65	5.0	V
V_{VDD}	Output Voltage	C_{VDD} = 1µF, Powering VDD from an external supply through BIAS (VBIAS>7V)		4.5	4.85	5.2	V
VBIAS	BIAS Operating Voltage Range			7		20	V
	VDD Regulator Input Switchover Threshold	Powering VDD from an external supply through BIAS			6.5	7	V

7. Typical specification, not 100% tested. Performance guaranteed by design and/or other correlation methods.

8. KTA1136 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continue)

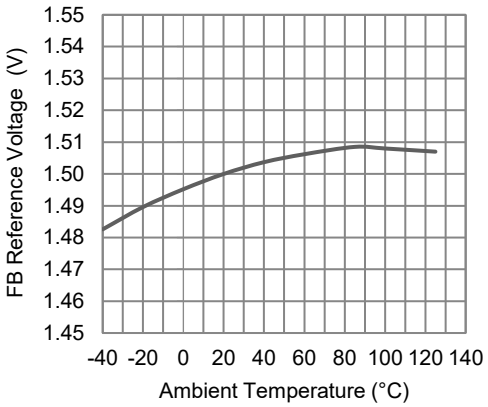
Unless otherwise noted, specifications are for T_A = -40°C to +85°C. Typical specifications are for T_A = +25°C and V_{IN} = 48V (at RJ45 Input). Typical specifications not 100% tested.

Symbol	Description	Conditions		Min	Typ	Max	Units
DC-DC Controller							
F_{OSC}	Oscillator Switching Frequency	R_{FSEL} = 392.0kΩ	All resistors ±1% Tolerance	80	100	120	kHz
		R_{FSEL} = 68.1kΩ		430	530	630	
		R_{FSEL} = 45.3kΩ		680	800	920	
$F_{OSC_\Delta T}$	Oscillator Temperature Coefficient	R_{FSEL} = 68.1kΩ ±1%			0.02		%/°C
D_{NDRV_MAX}	Maximum Duty Cycle	R_{FSEL} = 68.1kΩ ±1% (530kHz)			85		%
D_{NDRV_MIN}	Minimum Duty Cycle				6		%
V_{REF}	Error Amplifier Reference Voltage	Compared to input of the FB pin		1.47	1.5	1.53	V
Icss	Soft Start Pull-up Current				30		μA
I_{SOURCE}	Comparator Source Current	FB = 0V, COMP = 0V			60		μA
I_{SINK}	Comparator Sink Current	FB = 5V, COMP = 5V			80		μA
G_{ea}	Error Amplifier Transconductance				120		μS
R_{ea}	Error Amplifier Output Resistance				20		MΩ
F_{ea}	Error Amplifier Crossover Frequency				16		MHz
I_{FB_LEAK}	FB Leakage (source or sink)					100	nA
Switching Power MOSFET							
$R_{DSON\text{-}SW}$	Power MOSFET On Resistance				0.7		Ω
I_{LIM}	Power MOSFET Current Limit Threshold	RLIM = 130kΩ ±1%			1.7		A
Thermal Protection							
T_{J_TS}	Thermal Shutdown Temperature				160		°C
T_{J_HYS}	Thermal Shutdown Hysteresis				30		°C

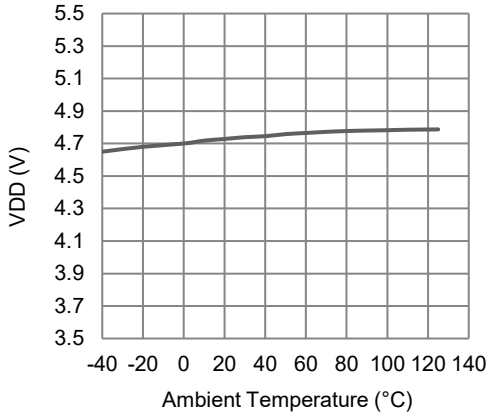
Typical Characteristics

V_{IN} = 48V (PSE Output), T_A = 25°C, F_{SW} = 530kHz, unless otherwise specified.

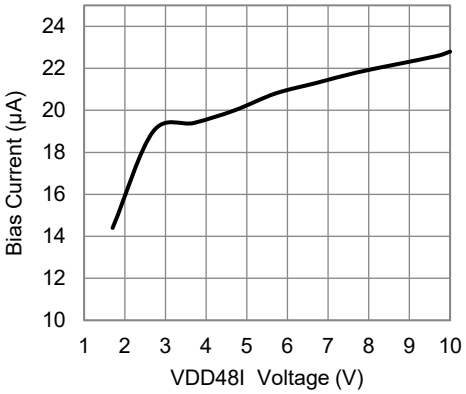
Reference Voltage vs. Temperature



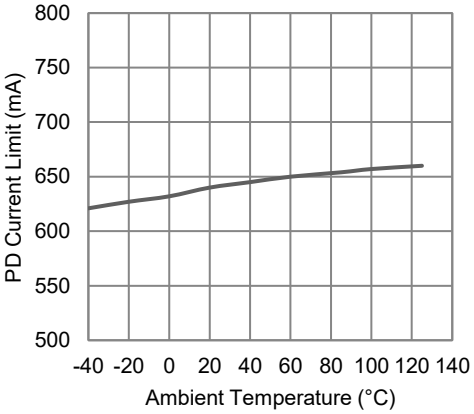
VDD vs. Temperature



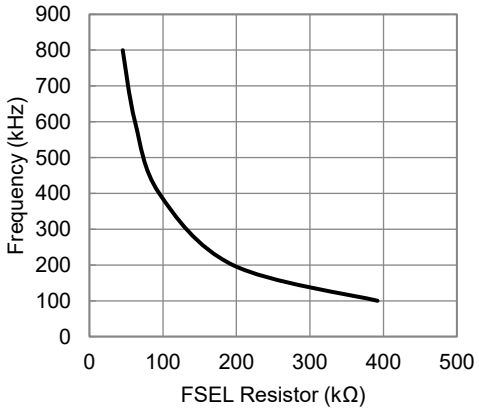
Detection Bias Current vs. Voltage



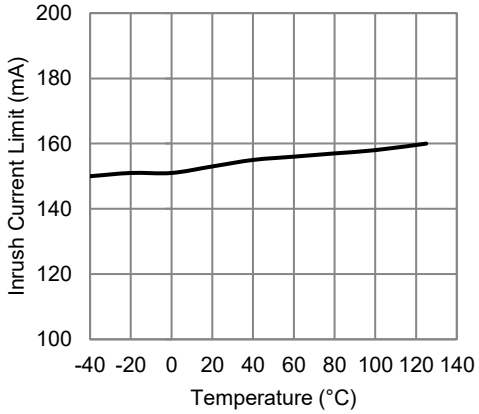
PD Current Limit vs. Temperature



Switching Frequency vs. FSEL Resistor



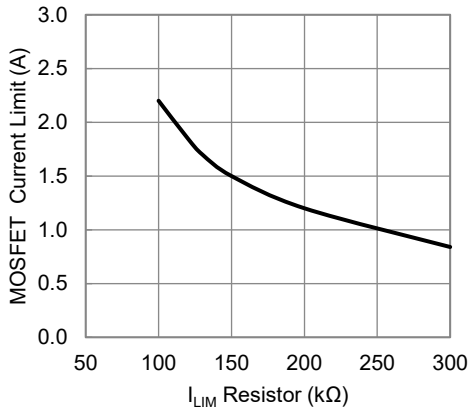
Inrush Current Limit vs. Temperature



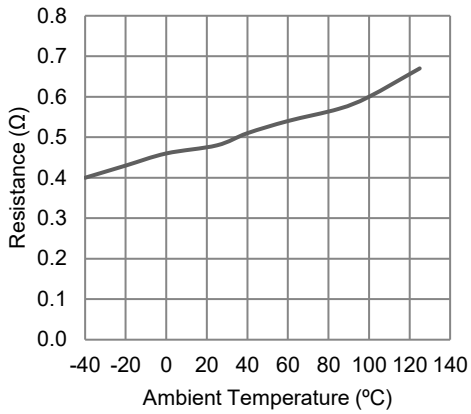
Typical Characteristics (continued)

V_{IN} = 48V (PSE Output), T_A = 25°C, F_{SW} = 530kHz, unless otherwise specified.

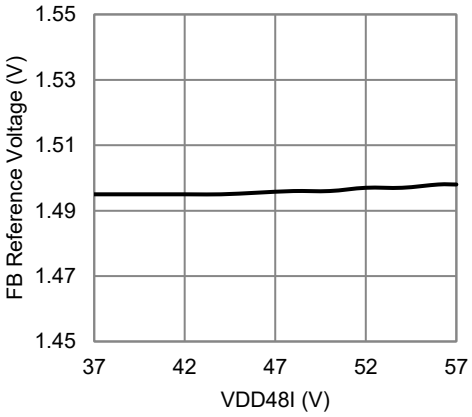
FET Current Limit vs. ILIM Resistor



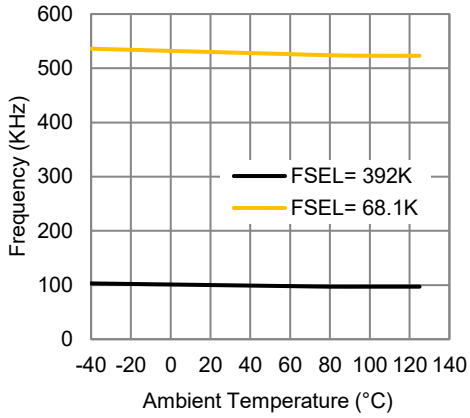
Hot-Swap FET Resistance vs. Temperature



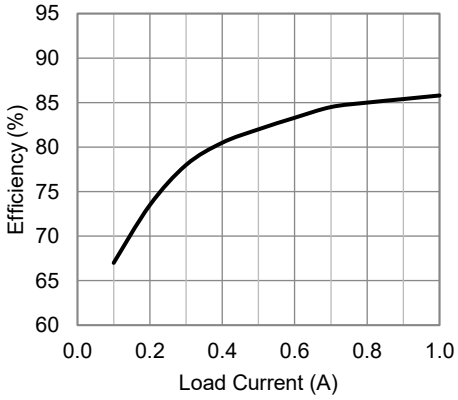
Reference Voltage vs. Input Voltage



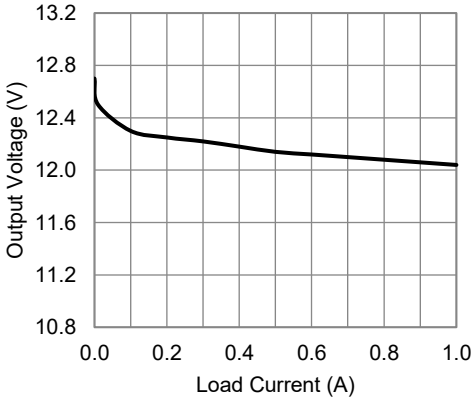
Switching Frequency vs. Temperature



Efficiency vs. Load Current



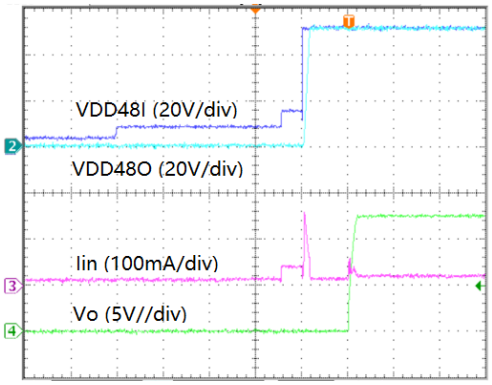
Output Voltage Load Regulation



Typical Characteristics (continued)

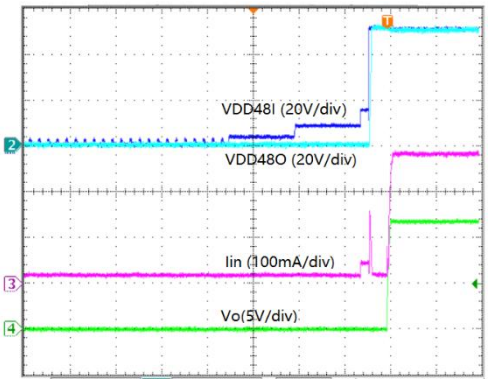
V_{IN} = 48V (PSE Output), T_A = 25°C, F_{SW} = 530kHz, unless otherwise specified. Device configured as an isolated primary side regulated power supply using an EP7 transformer.

Startup with PSE Input at 0A Load



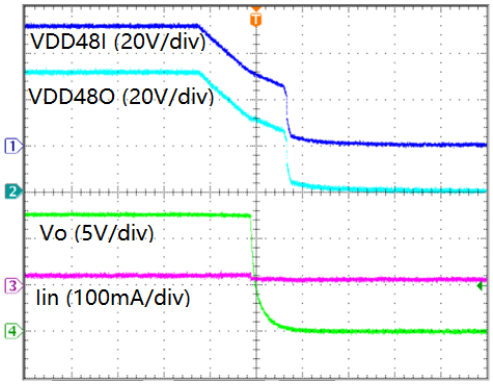
Time (40ms/div)

Startup with PSE Input at 1A Load



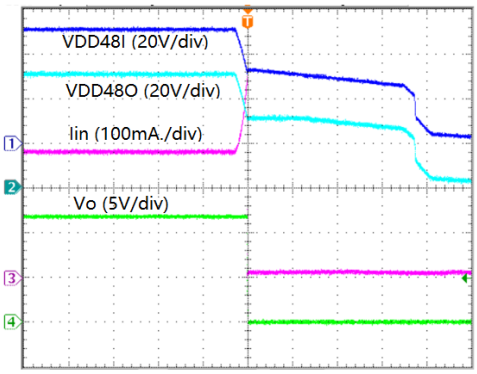
Time (100ms/div)

Shutdown by PSE at 0A Load



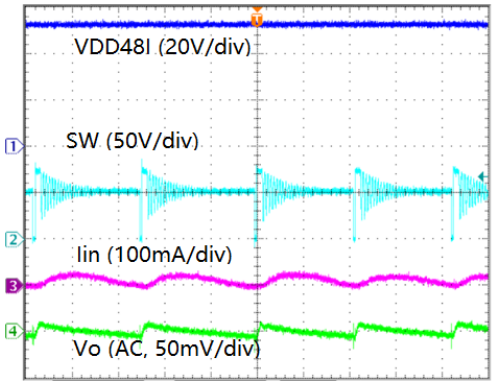
Time (400ms/div)

Shutdown by PSE at 1A Load



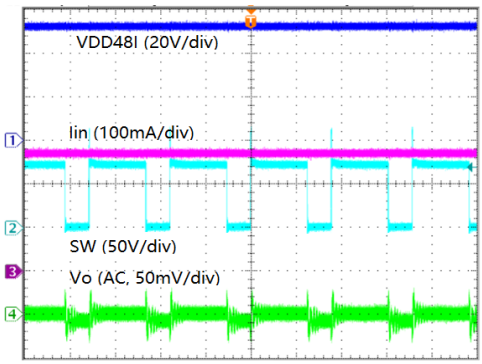
Time (100ms/div)

Steady State at 0A Load



Time (10µs/div)

Steady State at 1A Load

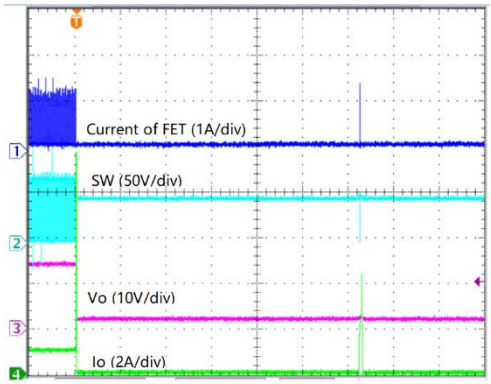


Time (1µs/div)

Typical Characteristics (continued)

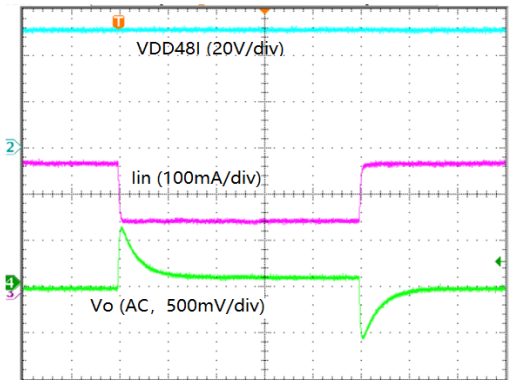
V_{IN} = 48V (PSE Output), T_A = 25°C, F_{SW} = 530kHz, unless otherwise specified. Device configured as an isolated primary side regulated power supply using an EP7 transformer.

SCP and Hiccup



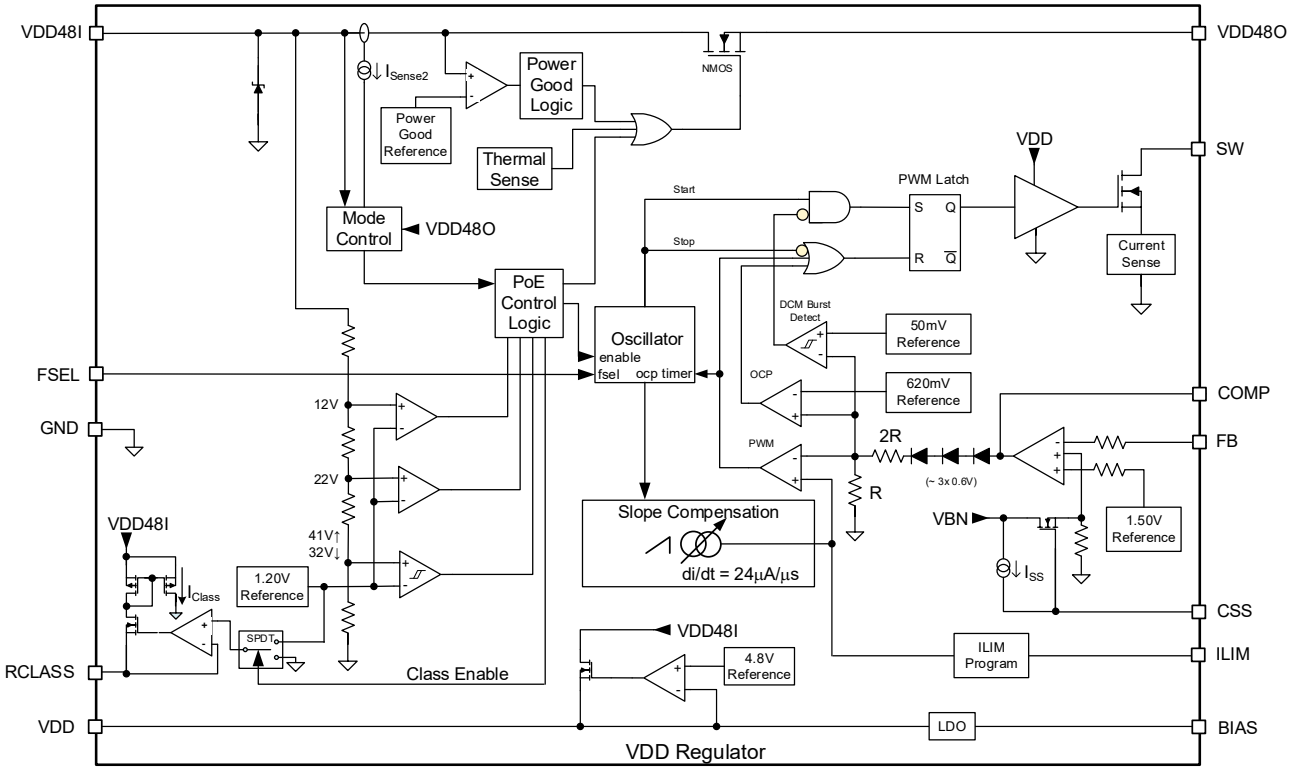
40ms / div

Load Transient (I_O = 0.5A to 1A, 25mA/µs)



2ms / div

Functional Block Diagram



Functional Description

Overview of PoE

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances, such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). PoE standards IEEE Std. 802.3af, 802.3at and 802.3bt are intended to unify the delivery method of usable power over Ethernet cables to remotely powered client devices. These standards define a method for detecting and querying PDs and then supplying a range of current levels based on the power class the device belongs to. By employing this method, designers can create systems that predict and minimize power usage, allowing the maximum number of devices to be supported on a powered Ethernet network.

The IEEE Std. 802.3 specification has evolved since its inception, gradually increasing the power level, but always remaining backwards compatibility with the previous revision.

The power source that provides current through the Ethernet cables to remote devices is referred to as the Power Sourcing Equipment (PSE). The powered device (PD) on the other end of the Ethernet cable negotiates for and receives the agreed-upon power. IEEE Std. 802.3af-2005 limits PSE power delivery to <13W at the PD input (Type 1 PD). IEEE 802.3at-2009 allows for >13W <30W power levels (Type 2 PD). IEEE 802.3bt-2018 allows for >30W <90W power levels (Type 3 & 4 PD).

The PSE uses the following IEEE 802.3af sequence to detect a connected PD, determine how much power it requires and then initiate supply current to the device:

- **Reset** — Power is withdrawn from the PD if the applied voltage falls below a specified level.
- **Signature Detection** — The PSE detects and evaluates whether the PD is a valid PoE device.
- **Classification** — The PSE reads the power requirement of the PD. The Classification level identifies how much power the PD will require from the Ethernet line. This permits optimum use of the total power available from the PSE. Classification is considered optional by IEEE standard 802.3af-2005 but IEEE standard 802.3at-2009 and 802.3bt-2018 requires Type 2 PSE to classify the PD for mutual identification.

- **On** — Operational state, during which the PSE provides the allocated power level to the PD.

This sequence occurs as a progressively rising voltage level from the PSE. It is designed to prevent high voltages from being present on an Ethernet line that does not have a valid PD attached (for user and non-PoE device safety).

To design PoE systems according to IEEE® standards, the following constraints apply:

Table 1. PoE Requirements

Requirement	Value
Maximum Type 1 PD input power	12.95W
Maximum Type 2 PD input power	25.5W
Maximum Type 3 PD input power	51W
Maximum Type 4 PD input power	71.3W
Output voltage from Type 1 PSE	44-57V
Output voltage from Type 2 PSE	50-57V
Output voltage from Type 3 PSE	50-57V
Output voltage from Type 4 PSE	52-57V
Minimum operating current limit, Type 1 @ PSE min output voltage	350mA
Minimum operating current limit, Type 2 @ PSE min output voltage	600mA
Minimum operating current limit, Type 3 @ PSE min output voltage	600mA
Minimum operating current limit, Type 4 @ PSE min output voltage	960mA
Line resistance, Type 1 operation	20.0Ω
Line resistance, Type 2,3 & 4 operation	12.5Ω
Input voltage at Type 1 PD interface	37.0V-57V
Input voltage at Type 2 PD interface	42.5V-57V
Input voltage at Type 3 PD interface	42.5V-57V
Input voltage at Type 4 PD interface	41.1V-57V

KTA1136 Design

To help designers meet these requirements, the KTA1136 is a fully integrated PoE PD regulator for Type1 PD implementations. The KTA1136 meets all system requirements for the IEEE 802.3af-2005 standard for Ethernet and all power management requirements for IEEE standard 802.3at-2009 and IEEE standard 802.3bt-2018 Type 1 PoE.

The KTA1136 integrates input surge protection, a PD controller with a hot-swap FET, a DC-DC controller, and a robust 150V switching power MOSFET. The KTA1136 acts as an interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. External diode bridges protect against polarity reversal, to provide alternative A and B detection.

The KTA1136 also passes the 8kV Contact Discharge and 15kV Air Discharge requirements, tested per IEC 61000-4-2. EMI compliance of KTA1136-based designs has been verified for CISP22 and FCC Class-B radiated and conducted emissions.

KTA1136 Overview

The KTA1136 is a fully integrated PD that provides the functionality required for Power-over-Ethernet (PoE) applications. The optimized architecture reduces external component cost in a small footprint while delivering high performance.

Rectification and Protection
To protect against polarity reversal, an external diode bridge is required. In conjunction with the external diode bridge, the KTA1136 provides over-voltage and transient protection on the line side of the Hot-Swap FET.

The KTA1136 is implemented in a robust 100V process technology. By integrating robust input protection circuitry, Kinetic has produced a solution that provides much faster response to surge events. The design also limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device and enables low-impedance safe discharge paths directly to earth ground. The protection circuit has been carefully designed to ensure that during these surge events, where currents can reach as high as 30A, voltages do not exceed critical breakdown and spark gap limits, protecting the PD from damage by the event. This enables system designers to achieve 15kV/8kV Air/Contact Discharge system ESD performance.

PD Controller
The KTA1136 PD Control Interface is designed to provide full PD functionality for IEEE® 802.3afcompliant systems, with programmable support for standard PD control functions.

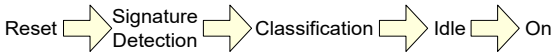
The PD Controller provides the following major functions:

- A resistance/capacitance connection path for the detection signature.
- Classification current for power classification.
- Full 13Watt PD supply capability
- Power management and thermal protection override, including UVLO (Under Voltage Lock Out).

Modes of Operation
The KTA1136 has five operating modes:

1. **Reset** — all blocks are disabled.
2. **Detection** — the external PD detection signature resistance / capacitance components are applied across the input.
3. **Classification** — PD indicates power requirements to the PSE via a Single-Event Classification for 802.3af.
4. **Idle** — this state is entered after Classification and remains until full-power input voltage is applied.
5. **On** — The PD is enabled, and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the KTA1136 transitions through the modes of operation in this sequence:



If no PSE is present, line voltage will be zero, which will hold the KTA1136 in the Reset state. The KTA1136 does not affect the Ethernet link function.

Reset
When the voltage supplied to the KTA1136 drops below the minimum valid detection voltage (i.e. <2.7V), the chip will enter the Reset state. While in Reset, the power supply to the PD is disconnected, the KTA1136 consumes very little power and the device reverts to the pre-detection status.

Detection Mode
During the detection sequence, the PSE applies a voltage to the PD to read its detection signature. The reading of the signature determines if a PD is present.

During detection, the PSE applies two sequential voltages, 1V or more apart, within the detection voltage range of 2.7V to 10.1V. It extracts a detection signature resistance value from the incremental I-V slope. Valid I-V slope resistance values are between 23.75kΩ and 26.25kΩ.

With the KTA1136, detection signature resistance is generated by an external resistor connected between VDD48I and GND. Typically this is a 25.5kΩ, ±1% resistor. With this value of RSIGNATURE, the PSE normally detects a total effective signature resistance of approximately 25kΩ, which is centered within the 802.3af/at specification range of 23.75kΩ to 26.25kΩ.

Valid PD detection also requires a valid detection signature capacitance of 0.05µF to 0.12µF at 2.7V to 10.1V, and 1.9V maximum offset voltage, per the IEEE 802.3af/at standard, measured at the PD input connector. KTA1136 detection signature capacitance is generated by an external 0.068µF capacitor connected between VDD48I and GND. The offset voltage is mainly provided by the external diode bridge voltage drop.

Classification Mode

Each class represents a power allocation range for a PD to assist the PSE in managing power distribution. IEEE Std. 802.3 defines classes of power levels for PDs, listed in Table 2.

If a PSE is Type 1, to classify the KTA1136, the Type 1 PSE presents a voltage between 14.5V and 20.5V to the PD and determines its class by measuring the resulting PD load current.

The KTA1136 allows the user to program the classification current via an external resistor connected to the RCLASS pin. Current, power levels and programming resistor values for each class are shown in Table 2. Note that for Class 0, RCLASS pin needs to be Pulled Up to VDD5 pin. This can be a direct short to VDD5 or using a resistor up to 100kΩ.

Use the following equation to determine the typical classification current:

$$I_{Class}[mA] = 2.0 + \frac{2360}{R_{Class}[k\Omega]} \quad (1)$$

Tolerance = Maximum of ±1.8mA or ±9%

R_{CLASS} > 63.4kΩ

Please note above class current expression haven't include the extra current flow the external detection resistor (typical 25.5kΩ), please add this extra detection current when do the class current calculation.

Once the classification process is done, the PD removes the classification current to conserve power.

Table 2. Classification Settings

Class	Power (W)	I_{CLASS} (mA)	R_{CLASS} (kΩ)
0	0.44-12.95	0 - 4	Pull-up (0-100kΩ) to VDD5 pin
1	0.44-3.84	9 -12	301kΩ, ±1%
2	3.84-6.49	17 – 20	147kΩ, ±1%
3	6.49-12.95	26 - 30	90.9kΩ, ±1%

Idle Mode

After the classification process, the PD enters Idle mode while it waits for On-state power delivery from the PSE. PD Current usage is limited to monitoring circuitry to detect the On-state voltage threshold.

On State

In the ON state, the KTA1136 is supplying power across the Ethernet line(s) to the PD. At a voltage at or above 37V, the PD turns on and full power is available via the KTA1136 DC-DC Controller.

PD Controller Power and Thermal Protection

The KTA1136 provides the following PD controller power and thermal protection:

- Under Voltage Lock Out (UVLO)
- Inrush Current Limit with integrated current sense
- Thermal Limit / Protection

Under Voltage Lock Out (UVLO)

The KTA1136 contains line Under-Voltage Lock Out (UVLO) circuitry to determine when to power on the PD. If the PSE supply voltage at PD PI is equal or greater than UVLO VIN_RISING, the KTA1136 PD will power on and run; if the PSE supply voltage at PD PI drops below UVLO VIN_FALLING, the KTA1136 PD will power off. The PD circuit controls power flow to the DC-DC controller, to protect the PD from erratic operation or damage.

Inrush Current Limit / Current Sense

Inrush limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges. This also prevents the PSE from going into current limit mode. The Current Limit/Current Sense circuitry also minimizes the PD on-chip temperature peaks by limiting both inrush and operating current.

Current is monitored with an integrated sense circuit that regulates the gate voltage on an integrated low-leakage power MOSFET. The power MOSFET can also be shut off completely by either the PD Controller or the Thermal Limit Protection circuitry.

During the PD startup sequence, VDS across the Hot-Swap FET is momentarily high as the VDD48O output capacitance is charged up, as illustrated in Figure 1 below. During this state, the Hot-Swap FET experiences a high instantaneous power drop and heating. Therefore, it is recommended that during this startup sequence, the incoming current should only be utilized for the charging of the VDD48O node, to minimize the startup time and associated power drop across the FET. The primary PWM controller is designed to accommodate for VDD48O startup before drawing power from the line. However, if the application requires direct use of the VDD48O node for other functions, the startup of those circuits should be delayed until the VDD48O node has reached its full voltage level.

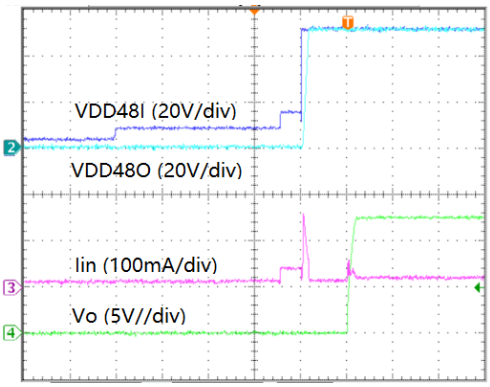


Figure 1. PI Input Voltage and Current

Thermal Limit / Protection

The KTA1136 provides thermal protection by the continuous monitoring of the die temperature. Thermal protection is triggered when the die temperature reaches 160°C, immediately turning off both the hot-swap MOSFET and DC-DC output MOSFET. When the die temperature falls below 130°C the hot-swap MOSFET and DC-DC output MOSFET will be turned on again.

PoE Power-On Startup Waveform

Figure 2 represents the power-on sequence for 2-Event PoE operation as outlined in IEEE 802.3at (IEEE 802.3bt specifies up to 5 multiple events). The waveform reflects typical voltages present at the PD during signature, classification and power-on.

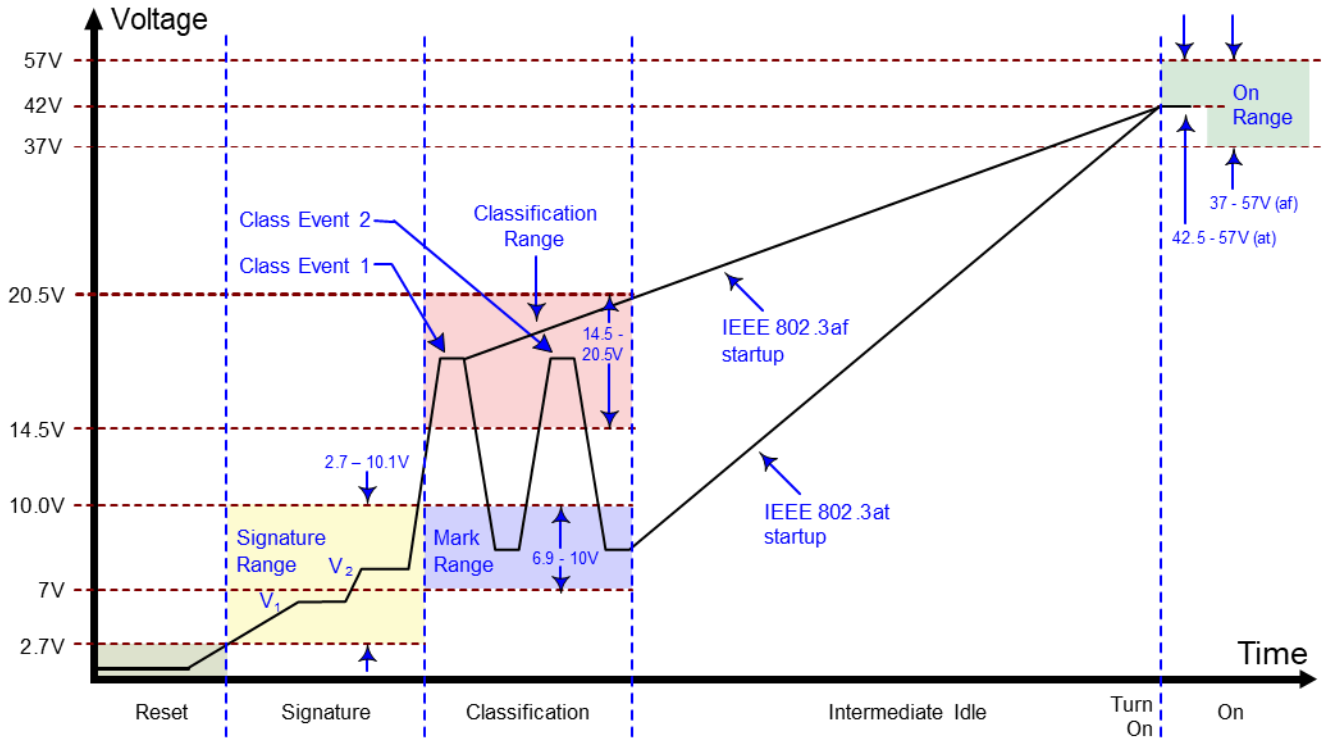


Figure 2. 802.3at Typical Power-On Waveform

1. Voltages V1 and V2 are applied by the PSE to extract a signature value.
2. The PSE takes current/impedance readings during Class/Mark Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistance connected to the RCLASS pin.
3. After the PSE measures the PD load current, if it is a high-power PSE, it presents a mark voltage (6.9V-10V), followed by a second classification voltage. The PD responds by presenting a load current as determined by the resistor on the RCLASS pin. After the PSE measures the PD load current the second time and determines that is can deliver the requested power, it moves into the On state by raising the voltage to approximately 42V.

DC-DC Regulator

Overview

The DC-DC architecture is a current-mode controller with integrated 150V output MOSFET, configurable with external components to fly-back, forward or buck topologies. Both non-isolated and isolated topologies are supported with either opto-coupled feedback.

As part of a full system-level solution to control EMI, Kinetic has focused significant attention on reducing switching noise in the integrated power converters through unique methods of shaping FET driver waveforms. Ground bounce is also reduced by minimizing dV/dt switching noise.

The integrated DC-DC controller operates from a switched input voltage (VDD48O) and includes a programmable soft start and current limiting. Once input power is applied and enable signals are asserted, the DC-DC controller starts-up switching the integrated output MOSFET and sensing the primary current in the

transformer. It also provides for an 80% maximum duty cycle, programmable PWM switching frequency and a true voltage-output error amplifier.

Programmable PWM Frequency
The FSEL pin allows the DC-DC converter switching frequency to be set externally. Placing a resistor between FSEL and GND sets the internal oscillator's frequency.

Table 3 identifies the resistor values for some commonly used switching frequencies.

Table 3. PWM Switching Frequency Selection

Switching Frequency (kHz)	FSEL Resistor (kΩ, ± 1%)
100	392
220	182
530	68.1
800	45.3

Current-Limit/Current Sense
The DC/DC regulator provides cycle-by-cycle current limit monitoring. The current limit is programmed via the resistor of ILIM pin. The DC/DC controller also provides short-circuit current protection. The DC/DC regulator will enter hiccup mode when peak current of primary FET reaches the programmed current limit point for several cycles.

Low Load Current Operation
The internal circuitry detects a low output power condition and puts the DC-DC Regulator into a discontinuous operation mode (DCM burst). Burst mode operation occurs when the COMP pin voltage drops below ~ 2.00V.

Compensation and Feedback
For isolated applications, loop compensation and output voltage feedback is generally provided by an opto-isolator circuit, and the Feedback pin (FB) is tied to ground. In these applications, the COMP pin is pulled up to approximately 4.8V by an internal current source. This pull-up can be the termination for an opto-isolator, or an additional resistor can be used in parallel.

For non-isolated applications, a resistive divider network, connected directly to the FB pin, senses the output voltage. The internal error amplifier is connected to a 1.5V reference voltage and the control loop will servo the FB pin to this voltage. A capacitive/resistive network connected to the COMP pin provides loop compensation.

Soft-Start
A capacitor is required on the CSS pin and is used to provide a controlled application power supply startup. At device power on, the capacitor on the CSS pin is slowly charged by an internal 30μA current source. The generated ramp voltage is used internally in the KTA1136 to provide soft-start for the regulator. The soft-start is finished when the generated ramp voltage around 1.2V on the CSS pin. For a 12V output Flyback design with PSR, a 100nF CSS capacitor will provide around 4ms of soft-start while 1μF CSS capacitor will provide around 40ms of soft-start.

Internal Switching FET
The SW and PGND provide connection to the drain and source of the integrated switching power MOSFET.

Power MOSFET its R_{DS_ON} is 0.7Ω. RCD snubber circuit for switching FET is suggested during operation. A recommendation RCD is to let the SW voltage of switching FET below 120V during normal operation.

The internal FET gate driver is powered from VDD voltage rail and the return path is through the GND pin.

Bias
It's an optional input to VDD bias regulator. Powering VDD from an external supply instead of VIN can reduce power loss at high VIN. For BIAS > 7V, the PVCC regulator draw current from BIAS pin. The BIAS pin voltage must not exceed 20V.

DC-DC Converter Application Topologies

The KTA1136 can be configured in several different isolated and non-isolated topologies. Like isolated Flyback and Non-isolated Buck topologies. The Buck topology is chosen for a non-isolated application. The Flyback mode is chosen for isolated application. When a minimum number of external components is desired, or there is a large step-down and the output voltage is typical over 5V. KTA1136 can be used as a secondary side regulation Flyback.

A typical Isolated secondary side regulation (SSR) Flyback design is shown in Figure 3. SSR application requires optocoupler and feedback components (voltage reference) on the secondary side. It has good regulation and good transient response compared with PSR application.

A typical Buck application design is shown in Figure **5**. Buck application is a low cost and high efficiency solution. Please note that the Ground for Vin and Vout is separate. If a common ground for Vin and Vout is requested, a more complicated DC-DC Converter topology like SEPIC can be used.

DC-DC Converter Design

Transform Design for Flyback

The transformer design is the most important part for flyback converter for secondary side regulation flyback application (refer Figure 3). Its design should consider the input voltage range, output voltage, and transform size. The key parameters of the transform are turn ratio, inductance, saturation current at a suitable size.

For the transform design, we usually design turn ratio first, then we design the inductance of transform, finally we design the saturation current of transform. Below are reference design procedure for a transform design (Continuous Current Mode), the transform parameters need a comprehensive consideration through turn ratio, inductance and saturation current, power MOSFET and diode voltage stress and so on.

Turns ratio is calculated as below expression 1.

$$n = \frac{Vin_min * Dmax}{(Vo_{max} + Vd) * (1 - Dmax)} \qquad \text{expression 1}$$

n : the turn ratio from winding to secondary winding

Vin_min : the min. operating input voltage

Vo_max : the max. output voltage

Vd : the forward voltage drop of secondary diode.

Dmax : max. duty cycle, for general, the max. duty cycle of the flyback converter is within 70%

For turn ratio, a typical 37Vin-57Vin PSE input range and 12Vo application, the recommended turn ratio(n) is around 2. A typical 37Vin-57Vin PSE input range and 5Vo application, the recommended n is around 5.

Inductance is calculated as below expression 2.

$$Lm = \frac{n*Vin*D*(1-D)}{Fsw*Io*Kc}$$ expression 2

Lm : the primary inductance of flyback transform

n : the turn ratio from primary winding to secondary winding

Vin : the operating input voltage

D : duty cycle.

Fsw : Switching frequency

Io : Output current

Kc : is the ripple current coefficient compared with output current, Kc is normally selected around 0.5 to 1.5 Inductance is mainly related to the switching frequency and transform size. In order to achieve a small total solution (refer Figure 3), a 530Khz high frequency transform is designed with EP7 Bobbin. It is only 1/3 volume size compared with traditional EP13 transform.

Peak current is calculated as below expression 3.

$$Ipeak = \frac{Io}{n*(1-D)} + \frac{Vin*D}{2Fsw*Lm}$$ expression 3

Ipeak: Primary peak current of the transform and internal switching MOSFET

Io: Output current

n : the turn ratio from primary winding to secondary winding

D : duty cycle

Vin : the operating input voltage

Fsw : Switching frequency

Lm : the primary inductance of flyback transform

This calculated peak current is the working current for the internal switching MOSFET and transform. The saturation current of the transform should be 30% larger than the peak current. The current limit of the internal MOSFET should also 30% larger than this peak current.

For a typical 37Vin-57Vin PSE input range and 12Vo flyback application, the recommended transform saturation current is around 2A. The current limit for the internal MOSFET is around 1.7A.

Output Inductor Design for Buck

The inductor design is important part for Buck converter application (refer Figure **5**). Its design should consider the input voltage range, output voltage, and inductor size. The key parameters of the inductor are inductance, saturation current at a suitable size.

Inductance is calculated as below expression 4.

$$Lm = \frac{(Vin - Vo) * D}{Fsw * Io * Kc}$$ expression 4

Lm : the inductance of output inductor

Vin : the operating input voltage

Vo : the output voltage.

D : duty cycle. The forward voltage drop of output power diode should be considered for a more accuracy duty cycle calculation.

Fsw : Switching frequency

Io : Output current

Kc : is the ripple current coefficient compared with output current, Kc is normally selected around 0.3 to 1.0 for Buck application. Io*Kc will get the peak current for the output inductor, output power diode and the internal MOSFET. The should have over 30% margin of this calculated peak current.

Inductor design is mainly related to the switching frequency, peak current and its size. For a typical 37Vin-57Vin PSE input range and 12Vo buck application (refer Figure **5**), the reference inductor design has a 47μH inductance and a 3A saturation current (10mm*10mm size).

Application Circuits

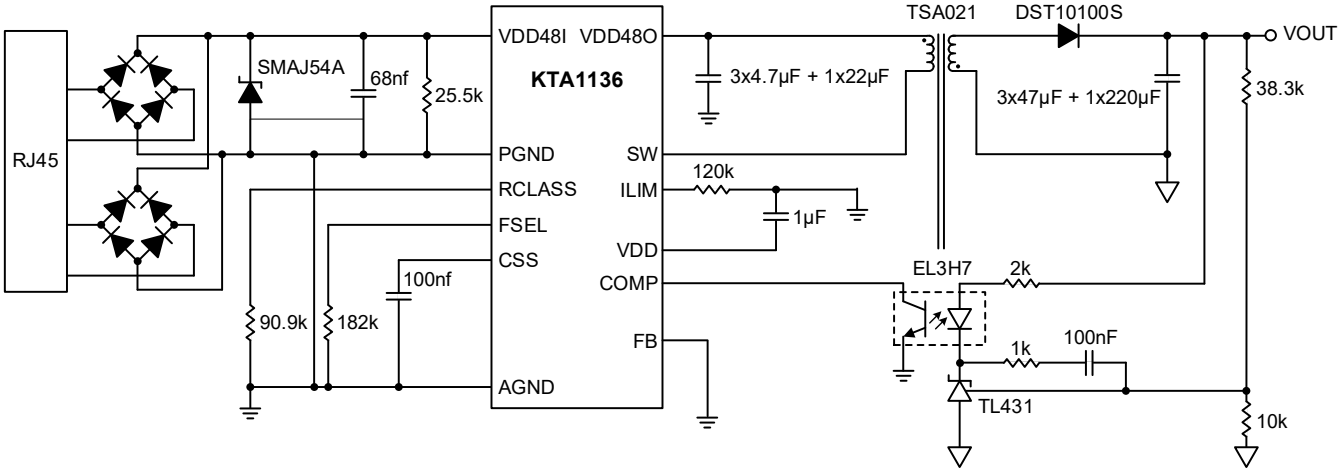


Figure 3. Flyback Application with Secondary Side Regulation

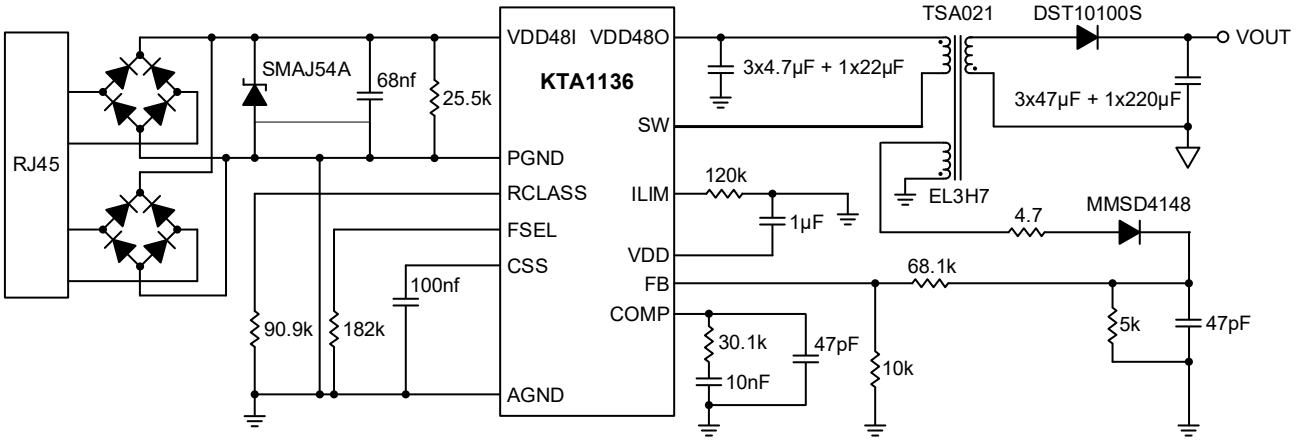


Figure 4. Flyback Application with Primary Side Regulation

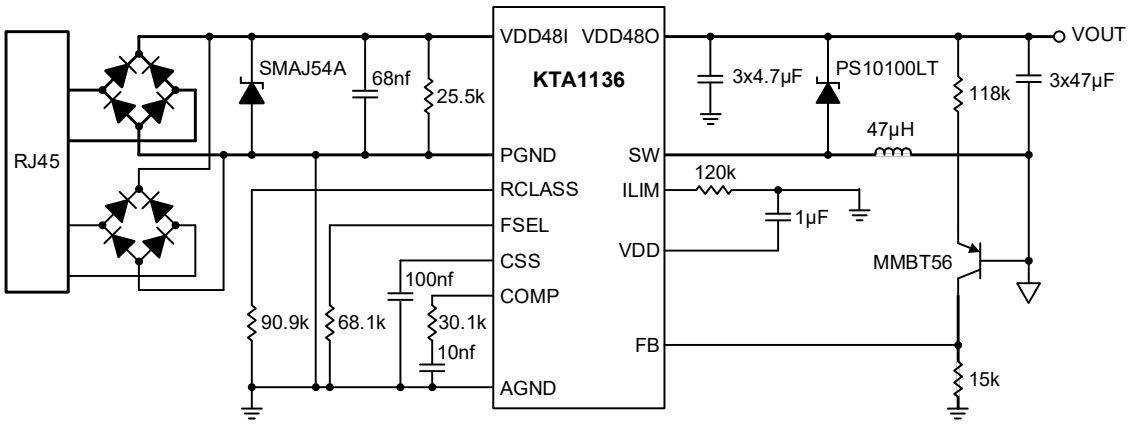
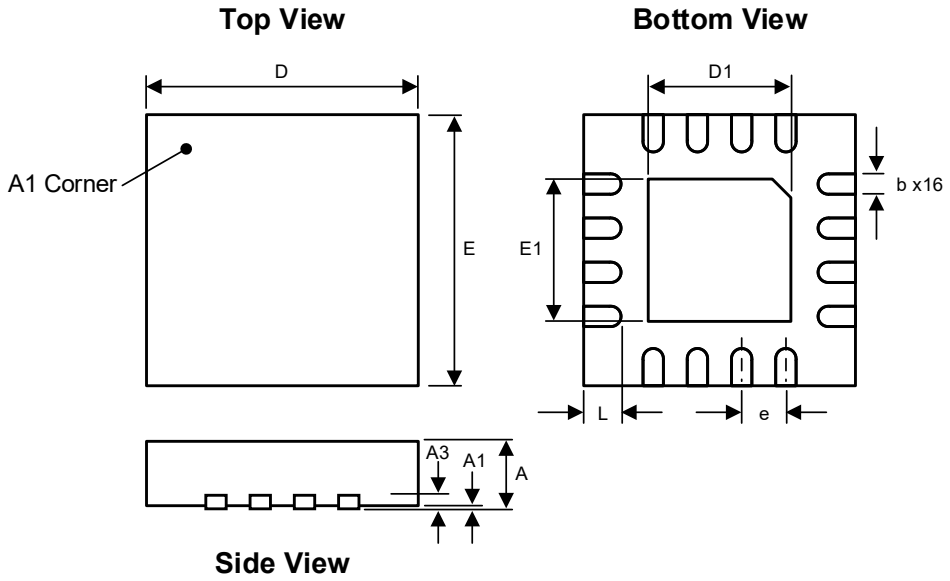


Figure 5. Simplified Buck Application

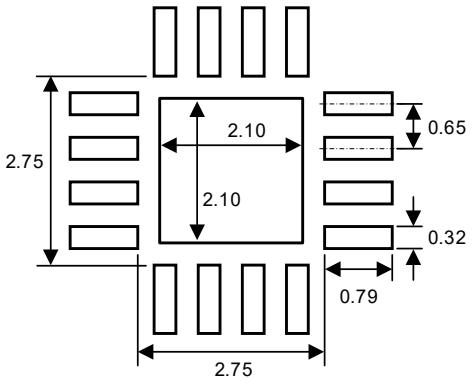
Packaging Information

TQFN44-16 (4.00mm x 4.00mm x 0.75mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.25	0.30	0.35
D	3.90	4.00	4.10
D1	2.00	2.10	2.20
E	3.90	4.00	4.10
E1	2.00	2.10	2.20
e	0.65 BSC		
L	0.50	0.55	0.60

Recommended Footprint



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