Application Note AN092

AS1434/1454 Software User's Guide

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FIGURES AND TABLES

ABOUT APPLICATION NOTE AN092

Application Note AN092 describes the software user interface for initializing, programming and monitoring the status of the Kinetic Technologies AS1434 and AS1454 devices. This document should be used in conjunction with the AS14x4 Datasheet for full understanding and usage of the device features and operating modes.

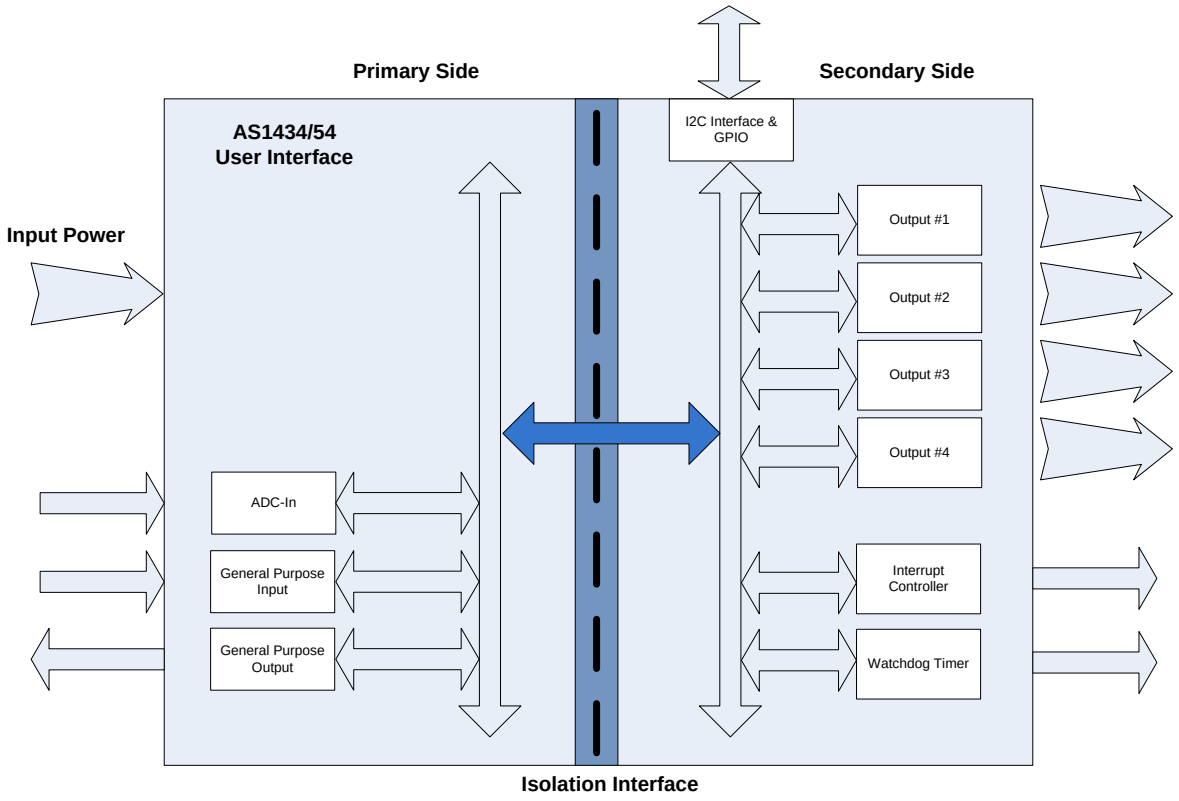
Refer to www.kinet-ic.com for further details on these and other Kinetic Technologies components.

SYSTEM OVERVIEW

The AS1434/AS1454 are quad-output DC-DC with integrated GreenEdge 2kV Isolation, supporting an input voltage range of 9-72VDC and 24VAC. This document describes the user interface for initializing, programming and monitoring the status of the AS1434/AS1454. For simplicity, the document refers only to the AS1454, but the user interface is identical for the AS1434. The system is divided into primary and secondary sides. The primary side contains the interfaces to the local power supply. The secondary side contains the four power outputs, as well as an interrupt controller, watchdog timer and I^2C control interface.

The two sides are isolated via the Kinetic *Digital Edge*™ isolation interface where digital and analog information can be transferred while maintaining electrical isolation.

Figure 1 - High-level Block Diagram of User Interface and Functional Blocks



I²C INTERFACE

Initialization, programming and monitoring are all accomplished through a fully compliant I²C interface on the secondary side of the isolation boundary. This interface operates at a maximum allowable clock frequency of 400KHz. The waveforms below show the basic operation of the I²C interface.

Figure 2 - I²C Start/Stop and Data Timing

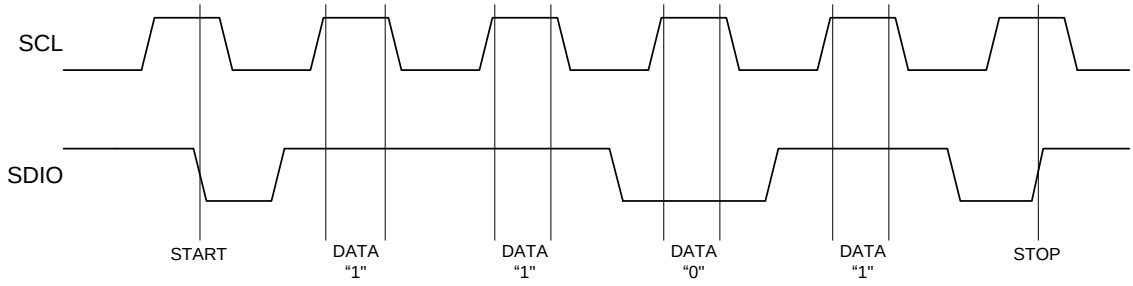
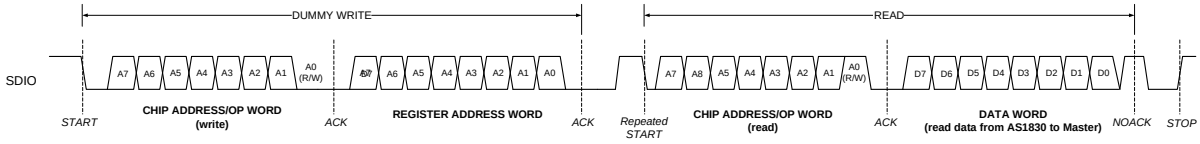


Figure 3 - I²C Write Cycle Timing

Figure 4 - I²C Read Cycle Timing



Address Decode

The AS1454 I²C interface is designed to inter-operate with other I²C devices which may be connected to the same wires. Distinction between I²C devices is done via the Chip Address/Op Word (see Figure 3 and Figure 4 above). The AS1454 is configured to respond to one of eight different chip-select addresses between 0b0100000x and 0b0100111x (the LSB determines read versus write).

Configuration of the chip-select address is determined by a resistor which is connected to the I2C_ADR1 pin on the primary side. The table below shows the chip-select address is determined by the I2C_ADR1 resistor value. The chip-select address must be unique from any other I²C device connected to the same interface (no other devices should respond to this device address) in order for the I²C interface to operate correctly.

Table 1 - I²C Device Address Setting from I2C_ADR1 Pin

Bit	Function	Description
A7	Fixed chip address bits	Internally fixed to 0
A6		Internally fixed to 1
A5		Internally fixed to 0
A4		Internally fixed to 0
A3	Configurable chip address bits	Chip address bits A3, A2 and A1 are configured by connecting a 1% resistor between pin I2C_ADR1 and ground (48N) as follows: 100KΩ· sets A3, A2, A1 = 1,1,1 86.6KΩ·sets A3, A2, A1 = 1,1,0 75.0KΩ·sets A3, A2, A1 = 1,0,1 61.9KΩ·sets A3, A2, A1 = 1,0,0 49.9KΩ·sets A3, A2, A1 = 0,1,1 37.4KΩ·sets A3, A2, A1 = 0,1,0 29.4KΩ·sets A3, A2, A1 = 0,0,1 12.4KΩ·sets A3, A2, A1 = 0,0,0
A2		
A1		
A0	$R/\overline{W}$	Specifies read or write operation

The second word transmitted as part of the I²C transaction contains the register address to be read or written. Reading/writing is determined by the LSB of the Chip Address/Op word. The AS1454 will respond to any address between the range 0x00 and 0xFF, but only supports registers in the range of 0x00 thru 0x0F.

AS1454 will respond to reads to addresses 0x10 thru 0xFF but the data will be undefined and should be ignored. The user should only write 0's to any register address from 0x10 thru 0xFF. Writing non-zero values to this register range can have unintended consequences, including damage to the AS1454 component or other components in the system.

Register Descriptions

The following table shows the high-level register map. Detailed descriptions of how these register bits are used follow the table.

Table 2 - User-accessible Register and Bit Summary

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
Interrupt Mask (INT MSK)	01	R/W	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Reserved
Interrupt Status (INT)	02	Read-Only	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Watchdog Timeout
PGOOD (PGD) Voltage Masks	03	R/W	Reserved	Reserved	Reserved	Output #4 Mask	Output #3 Mask	Output #2 Mask	Output #1 Mask	Reserved
Watchdog Enable, Mask, Service	04	R/W	Reserved	Reserved	Reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	Reserved	Reserved	Reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Time-out elapsed
Device Control and I/O Status	06	R/W	Reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	Reserved	Reserved	GPOP	GPIP
Watchdog Time-out	07	R/W	WDOG time-out counter (8 bits, in 125ms increments)							
A/D Voltage Read	08	Read-Only	ADCIN pin input voltage measurement (8 bits)							
A/D Alarm Threshold	09	R/W	Alarm Threshold for ADCIN (8 bits)							
System Clock Control	0A	R/W	Reserved				PWM Clock Modulate Enable	PWM Clock Modulate Type	PWM Clock Modulation Amount D1, D0	
Reserved	0B	Read-Only	Reserved							
Reserved	0C	Read-Only	Reserved							
Reserved	0D	R/W	Reserved							
Outputs 1,2 Voltage Margin Control	0E	R/W	Output #2 CCM/DCM Control	Output #2 Voltage Margin setting (D6, D5, D4)			Reserved	Output #1 Voltage Margin setting (D2, D1, D0)		
Outputs 3,4 Voltage Margin Control	0F	R/W	Reserved	Output #4 Voltage Margin setting (D6, D5, D4)			Output #3 CCM/DCM Control	Output #3 Voltage Margin setting (D2, D1, D0)		

GPIO

The AS1454 allows the user to send basic digital information across the isolation interface using the GPIO (General-Purpose I/O). The primary and secondary sides both have a general purpose input and output pin which can be used to send user-specific digital information across the isolation interface.

POWER OUTPUTS

The AS1454 has four power outputs which can be configured to deliver approximately 50W (AS1434 is approximately 20W) of power over a range of voltages. The AS1454 User's Guide is not intended to describe the analog configuration and behavior of these outputs. The configuration and operation of the power outputs is described in detail in the AS14x4 Design Guide and AS14x4 Datasheet.

The four power outputs can be individually controlled and adjusted via the I^2C interface. Gross adjustment is done externally via resistors and cannot be performed using the I^2C interface.

ADC

The AS1454 contains an ADC (Analog-to-Digital Converter) which provides the digitally encoded information of the absolute voltage being applied to the ADCIN input pin. The ADC input can be used for a user-specific analog measurement (e.g. temperature).

The ADC will provide a digital range of 0V to 2.55V in ~0.100V increments, with a 100Hz update rate. The AS1454 also supports a comparator to detect when the ADCIN voltage value crosses a threshold. Status and/or an interrupt can be generated for this event.
See section "ADC" on page 15 for a detailed description of the register interface and encoding scheme.

WATCHDOG TIMER

The AS1454 contains a programmable watchdog timer. This timer is programmable via a register. The 8-bit timeout value can be set from 0.125s to 31.875 seconds in 0.125s increments. Timeout behavior is also programmable. It can be programmed to generate a hardware interrupt or a power-good fault. It is fully controllable via the I^2C registers. See "Watchdog Timer Operation" on page 11 for details on how to program this feature.

INTERRUPT CONTROLLER

The AS1454 can be programmed to generate an interrupt (via the INTB pin or PGOOD pin) for many different events. Each interrupt event is individually and globally maskable. The possible interrupt events are:

- Watchdog Timer Timeout
- Over-temperature Alarm
- Over ADC-In Threshold Alarm
- Power-Good Fault On Any Power Output

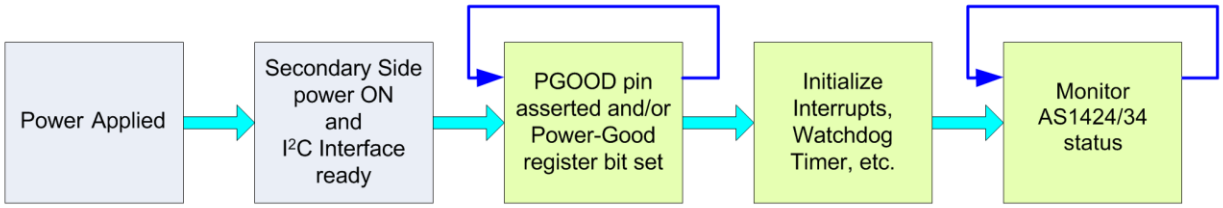
INITIALIZATION AND RESET

This section describes the power-up and initialization steps required.

POWER-UP

The diagram below describes the power-up sequence as seen by the user and should be used to help determine when power-up is complete and the system is stable.

Figure 5 - Power-Up Sequence



The AS1454 is defined as stable when all enabled power outputs are powered up and stable. This is indicated by the PGOOD pin being asserted high as well as bit 0 of register 0x00 being set to 0. One possible application of the PGOOD pin is as an active-low reset pin into the I^2C master. This guarantees that the I^2C master will not generate any transactions to the AS1454 until it is guaranteed to be stable and ready to receive transactions.

In a system where the PGOOD pin is not used to hold the I^2C master in reset, the I^2C master must poll the Global PGOOD Fault Bit (bit 0, register 0x00) continually until it is 0. All registers will be held in reset until the Global PGOOD Fault bit is 0.

RESET

A software reset can be performed to the secondary-side registers via bit 6 of register 0x06. This will reset the value of most registers back to their Reset value (as defined in Table 2). Note: Registers 0x04 and 0x05 are NOT reset by a software reset.

A software reset condition can also be caused by a PGOOD fault unless the PGOOD Reset Disable bit (bit 4 of register 0x06) is set or the corresponding PGOOD fault mask is set in register 0x03.

PROGRAMMING

Once power-up and initialization is complete, the I^2C interface can be used to set various programmable features such as interrupts, thresholds, and timeouts.

PROGRAMMABLE INTERRUPTS

The AS1454 can be programmed to allow certain events to generate a hardware interrupt to an external controller. Register 0x01 contains the interrupt mask controls for everything except the watchdog interrupt mask which is register 0x04. Setting any mask bit to a 0 in these registers disables interrupt generation for the corresponding condition. All interrupts are disabled at reset. The table below shows all the bits related to interrupt control. Bits not related are grayed out for clarity.

Table 3 - Registers Containing Interrupt Control Bits

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
Interrupt Mask (INT MSK)	01	R/W	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Reserved
Interrupt Status (INT)	02	Read-Only	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Watchdog Timeout
PGOOD (PGD) Voltage Masks	03	R/W	Reserved	Reserved	Reserved	Output #4 Mask	Output #3 Mask	Output #2 Mask	Output #1 Mask	Reserved
Watchdog Enable, Mask, Service	04	R/W	Reserved	Reserved	Reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	Reserved	Reserved	Reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Time-out elapsed
Device Control and I/O Status	06	R/W	Reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	Reserved	Reserved	GPOP	GPIP

In addition, the global interrupt enable (bit 5 register 0x06) must also be set to generate interrupts via the INTB pin (the INTB pin is open-drain and is driven low on assertion). If this global enable is not set, then the status bit for a given interrupt is still set, but no assertion is done on the INTB pin.

The interrupt service routine can read the interrupt status register to determine the cause of the interrupt. By reading the status register, all interrupt conditions are cleared, and the INTB pin is de-asserted. Register 0x00 also contains information on the related condition even when the interrupt mask is 0 for that condition.

POWER-GOOD FAULT SETTINGS (PGOOD GENERATION)

Each of the four power outputs has an individual power-good fault indicator located in bits [4:1] of register 0x05. PGOOD fault conditions are caused by an over-voltage, under-voltage condition, or a short-circuit condition on a specific power output. If one of these bits is set then that power-good has been low for at least (10 µs) for the corresponding power output. These values can only be cleared by writing a 0 to the desired location. Writing a 1 has no effect and will be ignored. Register 0x00 has a non-maskable status bit indicating a fault as well which can be used even if the interrupt is disabled. If the fault bit is cleared but the power-fault condition has not resolved itself, then the PGOOD fault bit will be set again in 10us or less. The table below shows registers bits related to PGOOD generation (bits not related are grayed out for clarity).

Table 4 - Registers with Bits Related to Power-Good

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
PGOOD (PGD) Voltage Masks	03	R/W	Reserved	Reserved	Reserved	Output #4 Mask	Output #3 Mask	Output #2 Mask	Output #1 Mask	Reserved
PGOOD & Watchdog History	05	R/W	Reserved	Reserved	Reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Time-out elapsed
Device Control and I/O Status	06	R/W	Reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	Reserved	Reserved	GPOP	GPIP

Register 0x03 can be programmed to individually mask out fault conditions from each power output. Setting a 1 for a given output will enable a PGOOD fault for that output. A PGOOD fault causes the external PGOOD pin to go low for at least 10ms. This can be used as another interrupt level if desired (e.g. a non-maskable interrupt).

In addition, a PGOOD fault can also be used to generate a software register reset if the Disable PGOOD reset (bit 4 of register 0x06) is not set. This reset will NOT reset registers 0x04 or 0x05. Note, in the case where a power output is externally disabled (see the AS14x4 Design Guide), it is guaranteed that the PGOOD fault for that power output will never assert. Therefore, the software can set the PGOOD fault mask for all power outputs even when certain outputs are disabled.

WATCHDOG TIMER OPERATION

The watchdog timer can be configured (via hardware) to automatically start at power-up or be disabled by default. This is done by either floating the WDOG_MODE pin (auto-start) or pulling the WDOG_MODE pin high (disabled). If configured for auto-start, the watchdog timer will timeout after approximately 32 seconds after the AS1454 reaches a stable "power-good" state.

If disabled by default, the watchdog timer must be enabled explicitly via the I^2C interface. Enabling the Watchdog Timer requires two consecutive I^2C operations: Setting Watchdog Enable (bit 4 register 0x04) along with the desired value of Watchdog Interrupt Mask, Watchdog PGOOD Mask and Watchdog Register Reset Mask bits, followed by a consecutive write to register 0x00 with the pattern 0xBB. Bits

[4:1] of register 0x04 cannot be set any other way, and cannot be changed (they are read-only) when Watchdog Enable is high, and do not change during a software reset. Note: This means that they can only be written to once after power up and cannot be modified after that. The values of bits [4:1] will not actually be set until the write of 0xBB to register 0x00 is completed.

Bits [3:1] of register 0x04 are use to set the behavior of the AS1454 when a timeout occurs. If bit 3 is set to 1, then an interrupt will be generated. If bit 2 is set a 1, then a timeout is treated like a Power-Good fault event and PGOOD will be pulled low (see Table 5). Finally if bit 1 is set to a 1, then the watchdog timeout will not cause a software reset of the register space.

In addition to the timeout behavior described above, the watchdog timer will normally reload to its start value and begin counting down again immediately. However, if the Watchdog Register Reset Mask (bit 1 of register 0x04) is not set, then the timer start value will be reset to 31.875 seconds instead.

To reset or service the watchdog timer prior to timeout, the Watchdog Service Control bit (bit 0, register 0) can be used. Servicing the Watchdog function via software requires two consecutive I^2C operations: First, a write to this register, setting the Service Watchdog bit, followed by a consecutive write to register 0x00 with the pattern 0xAA. The write to 0x00 must occur prior to the next timer timeout. Even at the minimum timeout period of 125ms, there should be ample time to perform two writes on the I^2C interface at 400KHz. Note that since register 0x00 is read-only, these extra writes will not alter the contents of the register.

Table 5 - Watchdog Timer

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Watchdog Enable, Mask, Service	04	R/W	Reserved	Reserved	Reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	Reserved	Reserved	Reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Time-out elapsed
Watchdog Time-out	07	R/W	WDOG time-out counter (8 bits, in 125ms increments)							

The timer duration is set in register 0x07. This is an 8-bit linear encoding in 125ms increments. The value 0x00 is reserved and should not be used. The value written to this register will take effect at the next watchdog timer timeout or watchdog servicing event.

For example:

- 0x01 = 125ms
- 0xFF = 31.875s

Example Watchdog Programming

1-second Timeout w/ Interrupt:

```
Write 0x07 => 0x07          ; 1 Second Timeout Value
Write 0x06 => 0b001x00xx    ; Ensure Interrupts Are Enabled
Write 0x04 => 0b00011010    ; Enable timer w/Interrupt, No PGOOD Fault, No Reg. Reset
Write 0x00 => 0xBB          ; Enable Timer
```

Service Routine To Reset Counter and load new timeout value to 10seconds:

```
Write 0x07 => 0x01001111    ; 10-second timer value
Write 0x04 => 0b000xxxx1    ; Set Service Bit
Write 0x00 => 0xAA          ; Reset Counter
```

ADJUSTMENTS AND MARGINING CAPABILITY

All four power outputs have individual voltage-margining capability for doing small adjustments to the voltage reference. These margin adjustments are located in bits [6:4], [2:0] of registers 0x0E and 0x0F. These 3-bit fields represent a +6% to -8% adjustment to voltage reference in 2% increments for outputs 2, 3, and 4. For output 1, they represent a +/- 5% adjustment, with a 2.5% resolution. See Table 7 for a code to % margin translation.

Table 6 - Margin Control

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Outputs 1,2 Voltage Margin Control	0E	R/W	Output #2 CCM/DCM Control	Output #2 Voltage Margin setting (D6, D5, D4)			Reserved	Output #1 Voltage Margin setting (D2, D1, D0)		
Outputs 3,4 Voltage Margin Control	0F	R/W	Reserved	Output #4 Voltage Margin setting (D6, D5, D4)			Output #3 CCM/DCM Control	Output #3 Voltage Margin setting (D2, D1, D0)		

Table 7 - 3-bit Voltage Reference Adjustment Encoding

Bits	Voltage Adjust Output 1	Voltage Adjust Output 2, 3, 4
000	0% (default)	0% (default)
001	-5%	2%
010	-2.5%	4%
011	2.5%	6%
100	5%	-8%
101	Reserved, do not use	-6%
110	Reserved, do not use	-4%
111	Reserved, do not use	-2%

SETTING LIMITS AND ALARMS

The user can set a threshold for a specific ADC voltage value which generates an alarm and interrupt. The ADC threshold value can be programmed to register 0x09. When the measured ADC-In voltage is greater than the threshold for more than approximately 3ms, the alarm bit in register 0x00 is set and an interrupt is generated, unless A/D Over Threshold Alarm is masked. See section "ADC" on page 15 for details on the encoding of the ADC value and threshold.

Table 8 - Alarms

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
Interrupt Mask (INT MSK)	01	R/W	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Reserved
Interrupt Status (INT)	02	Read-Only	Reserved	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Watchdog Timeout

In addition to the ADC-In voltage, the AS1454 also monitors temperature. The "Over-Temp Alarm" (bit 6, register 0x00) is set when the junction temperature measured of the AS1454 controller exceeds 145°C. If the junction temperature reaches 160°C, the AS1454 will shutdown. As with the voltage alarm, an interrupt will be generated unless masked.

MONITORING AND STATUS

Once the AS1454 has been configured for interrupts, thresholds and timeouts, the external controller should be able to go into a normal monitoring loop polling values (if desired) and waiting for any interrupts. The watchdog timer and its associated interrupt can be used as a way to periodically poll specific values such as ADC-In and General Purpose I/O values, as well as miscellaneous status information.

SAMPLING/UPDATE RATE CONSIDERATIONS

The update rate of status bits in the AS1454 differs according to which bits they are.

The following bits have negligible update latency:
Power good fault #1-4

The following bits have a worst case 4ms latency/update rate:
Temperature alarm,
LDET,
AT_DET,
CLIM
ADCIN voltage measurement,
PD input voltage measurement

Other than that, there are no special considerations.

ADC

Table 9 - ADC Register

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
A/D Voltage Read	08	Read-Only	ADCIN pin input voltage measurement (8 bits)							
A/D Alarm Threshold	09	R/W	Alarm Threshold for ADCIN (8 bits)							

The ADC-In (user ADC) value can be monitored via the 0x08 register. This register value represents a linear-encoded voltage on the ADCIN pin between 0V (0x00) and 2.55V (0xFF) in approximately 0.100V increments. If the voltage on the ADCIN pin exceeds 2.55V, the ADC will saturate at 0xFF.

The ADC-In threshold value, which can be used to cause an interrupt and alarm when exceeded, can be set by register 0x09. See Settings Limits and Alarms on page 14 for use.

All ADC register fields have an update rate of 100Hz (10ms period). The ADC subsystems on the primary side actually have an update rate of 1.5KHz, but the information is only transmitted at a 100Hz update rate.

GPIO SETTING AND POLLING

In software mode, there are no external GPIO pins on the secondary side. Setting GPIN and sensing the GPOUT on the primary side is done via register reads and writing to bits [1:0] of register 0x06. To set the value present on the GPO1 pin on the primary side, the value is written to bit 1 of register 0x06. The value present on the GPI1 pin on the primary side can be read from bit 0 of register 0x06.

EXAMPLE PSEUDO CODE

This section contains example pseudo code for initialization, programming, monitoring and servicing the AS1454. It is provided to clarify usage models, and is not intended to be considered the only way that software control can be implemented.

The example below is for a video camera with external light sensor and external light.

PSEUDO CODE CONVENTIONS

The following instruction words are used:

```
write <reg>, <data>           Write <data> (via I2C) to AS1454 register <reg>
$a=read <reg>                 Read data from AS1454 register (via I2C) and
store in symbol $a
//<comment>             Comment text
```

INITIALIZATION AND CONFIGURATION CODE

```
initialize()
      {
      //wait for power-good
      $a=1;
      while($a&0x01)
         {
         $a=read 0x01 //check global power-good fault bit
         }

      ////////////////////////////////////////////////
      //SETUP LIMITS and ALARMS                     //
      ////////////////////////////////////////////////
      //ADCIN being used for external light sensor
      //when value is > about 128, light is too low, to turn on ext. light
      write 0x09,0x80

      ////////////////////////////////////////////////
      //SETUP INTERRUPTS
      ////////////////////////////////////////////////
      //First, make sure interrupt status is cleared
      $int_status=read 0x02 //read clears status
      //Now enable interrupts for over temp to start with
      write 0x01, 0b01000000
      //Do not turn on INTB pin yet, wait until done with all setup

      ////////////////////////////////////////////////
      //SETUP HIGH-PRIORITY INTERRUPT (PGOOD)
      ////////////////////////////////////////////////
      write 0x03, 0b00011110  //Enable all 4 power-output fault indicators
      write 0x06, 0b00010000  //Disable reset on PGOOD,reset handled by sw
```

```
      ////////////////////////////////////////////////
      //SETUP WATCH DOG
      ////////////////////////////////////////////////
      //Enable timer and enable for interrupts, no reset of registers
      write 0x04,0b00011000
      write 0x00,0xBB ;special write required for last write to be registered
      //watchdog timer now running with default 32-second timer


      //Set timer value to 1 second
      write 0x07,0x08  ;1-second timeout
      //After Next Timeout timer will start 1-second timeout

      ////////////////////////////////////////////////////////
      //ENABLE INTERRUPTS
      ////////////////////////////////////////////////////////
      $dev_ctrl=read 0x06
      $dev_ctrl |= 0b00100000
      write 0x06, $dev_ctrl
      //interrupts now enabled
}

int_handler_routine()
   {
   $int_status=read 0x02;
   $over_temp=$int_status & 0x40;
   $over_adcin_thresh=$int_status & 0x20;
   $time_out=read 0x05 & 0x01;

   //not using pgood fault INT, not enabled
   $timeout = $int_status & 0x01;

   if($over_temp)
       {
       call severe_error_handler("Power System Failure: Temperature Too
High\n");
       call shutdown();
       }
   if($over_adcin_thresh)
      {
      $ext_light=1
      //Disable interrupt for ADCIN (light level)
      $monitor_light=1;
      $int_mask=read 0x01;
      $int_mask&=0xDF;  //Disable interrupt for ADCIN threshold alarm
      call ext_light_control($ext_light)
      }
    if($time_out)
       {
       $adc_in=read 0x08;
       call monitor_routine ($monitor_light, $adc_in);
       }
   }
```

```
hi_pri_int_handler_routine()
   {
   //This routine handles PGOOD de-assertions like a high-priority interrupt
   $pgood_status=(read 0x05) >>1;
   if($pgood_status)
      {
      call severe_error_handler("Power System Failure: Power Delivery Fault
Detected\n");
      call shutdown();
      }
   }


ext_light_control($ext_light)
   {
   //This routine controls an external light via the general-purpose IO
   //set GPOUT to turnon external light
   $dev_ctrl=read 0x06;
   $dev_ctrl|=0x02;
   write 0x06, $dev_ctrl;
   $light_on=0;
   //wait for light to actually turn on;
   //check GPIN
   while(! $light_on)
      {
      $light_on=(read 0x06&0x01);
      }
   }
```

CONTACT INFORMATION

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