Akros Silicon™
A Division of
Kinetic Technologies

Application Note AN082

AS1854/1834 Software User's Guide

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FIGURES AND TABLES

ABOUT APPLICATION NOTE AN082

Application Note AN082 describes the software user interface for initializing, programming and monitoring the status of the Kinetic Technologies AS1854 and AS1834 devices. This document should be used in conjunction with the AS18x4 Datasheet for full understanding and usage of the device features and operating modes.

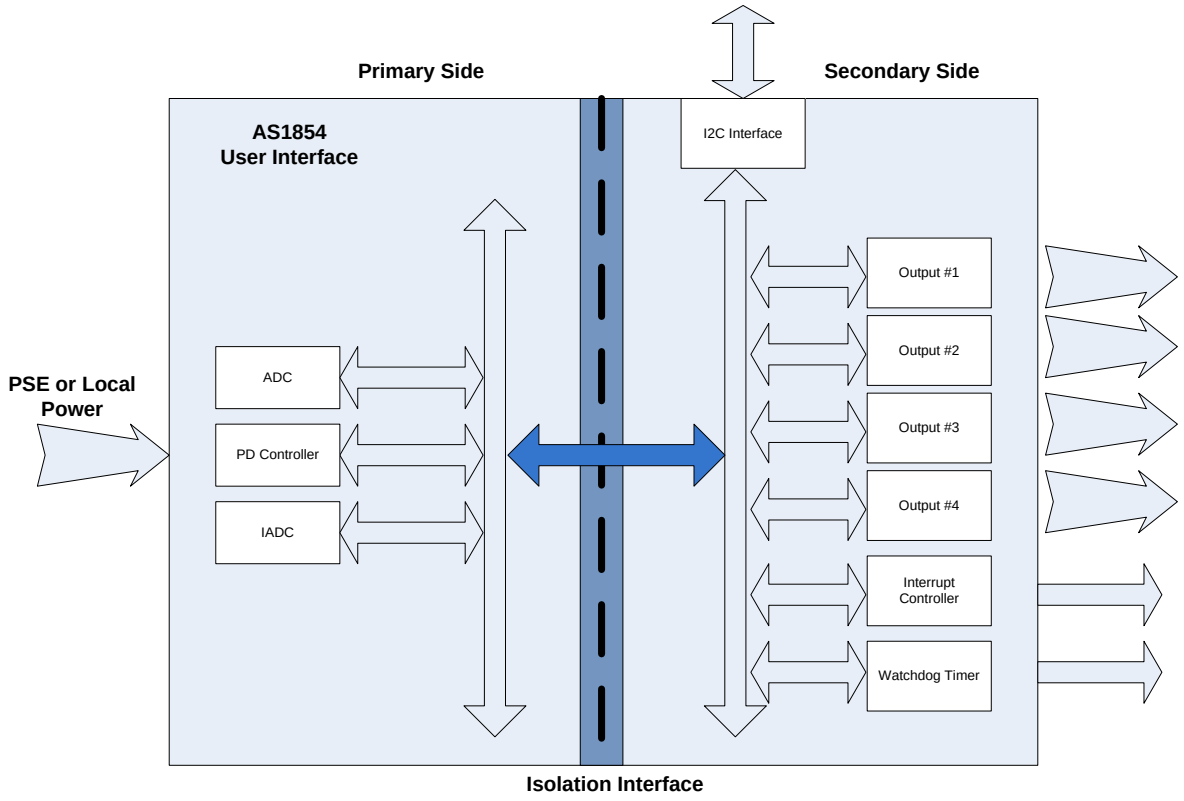
Refer to www.kinet-ic.com for further details on these and other Kinetic Technologies components.

SYSTEM OVERVIEW

The AS1854 is an IEEE802.3at/af-compliant PoE PD Controller and Isolation component for use in Type 2 PD applications. The AS1834 is IEEE802.3af compliant for use in Type 1 PD applications. This document describes the user interface for initializing, programming and monitoring the status of the AS1854 and AS1834. For simplicity, the document refers only to the AS1854, but the user interface is identical for the AS1834. The system is divided into primary and secondary sides. The primary side contains the PD controller and interfaces to the PSE or local power supply. The secondary side contains the four power outputs, as well as an interrupt controller, watchdog timer and I^2C control interface.

The two sides are isolated via the Kinetic *Digital Edge*™ isolation interface where digital and analog information can be transferred while maintaining electrical isolation.

Figure 1 - High-level Block Diagram of User Interface and Functional Blocks



I²C INTERFACE

Initialization, programming and monitoring are all accomplished through a fully compliant I²C interface on the secondary side of the isolation boundary. This interface operates at a maximum allowable clock frequency of 400KHz. The waveforms below show the basic operation of the I²C interface.

Figure 2 - I²C Start/Stop and Data Timing

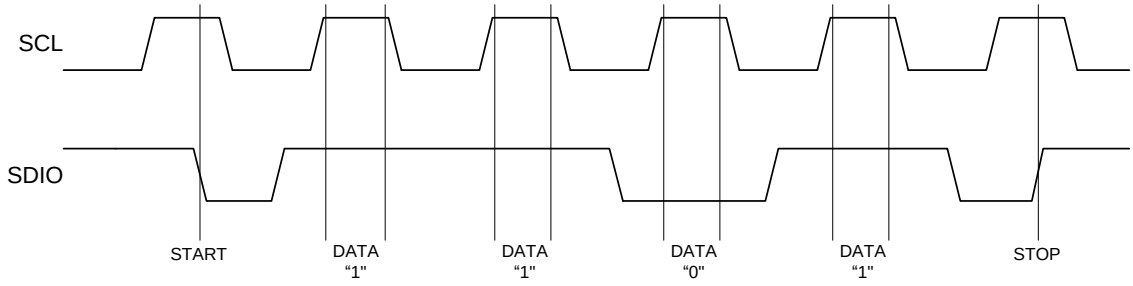
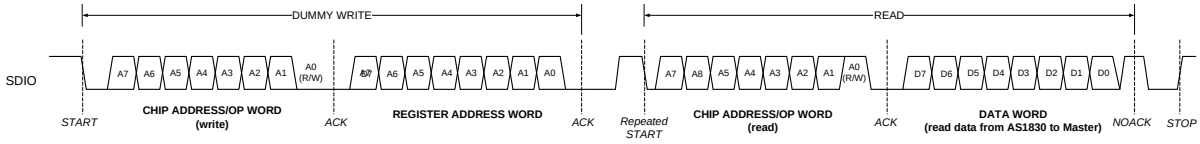


Figure 3 - I²C Write Cycle Timing

Figure 4 - I²C Read Cycle Timing



Address Decode

The AS1854 I²C interface is designed to inter-operate with other I²C devices which may be connected to the same bus. Distinction between I²C devices is done via the Chip Address/Op Word (see Figure 3 and Figure 4 above). The AS1854 is configured to respond to one of eight different chip-select addresses between 0b0100000x and 0b0100111x (the LSB determines read versus write).

Configuration of the chip-select address is determined by a resistor which is connected to the I2C_ADR1 pin on the primary side. The table below shows the chip-select address is determined by the I2C_ADR1 resistor value. The chip-select address must be unique from any other I²C device connected to the same interface (no other devices should respond to this device address) in order for the I²C interface to operate correctly.

Table 1 - I²C Device Address Setting from I2C_ADR1 Pin

Bit	Function	Description
A7	Fixed chip address bits	Internally fixed to 0
A6		Internally fixed to 1
A5		Internally fixed to 0
A4		Internally fixed to 0
A3	Configurable chip address bits	Chip address bits A3, A2 and A1 are configured by connecting a 1% resistor between pin I2C_ADR1 and ground (48N) as follows: 100KΩ· sets A3, A2, A1 = 1,1,1 86.6KΩ·sets A3, A2, A1 = 1,1,0 75.0KΩ·sets A3, A2, A1 = 1,0,1 61.9KΩ·sets A3, A2, A1 = 1,0,0 49.9KΩ·sets A3, A2, A1 = 0,1,1 37.4KΩ·sets A3, A2, A1 = 0,1,0 29.4KΩ·sets A3, A2, A1 = 0,0,1 12.4KΩ·sets A3, A2, A1 = 0,0,0
A2		
A1		
A0	$R/\overline{W}$	Specifies read or write operation

The second word transmitted as part of the I²C transaction contains the register address to be read or written. Reading/writing is determined by the LSB of the Chip Address/Op word. The AS1854 will respond to any address between the range 0x00 and 0xFF, but only supports registers in the range of 0x00 thru 0x0F.

AS1854 will respond to reads to addresses 0x10 thru 0xFF but the data will be undefined and should be ignored. The user should only write 0's to any register address from 0x10 thru 0xFF. Writing non-zero values to this register range can have unintended consequences, including damage to the AS1854 component or other components in the system.

Register Map

The following table shows the high-level register map. Detailed descriptions of how these register bits are used follow the table.

Table 2 - User-accessible Register Bit Map

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
Interrupt Mask (INT MSK)	01	R/W	Over-Current Alarm INT MSK	Over-Temp Alarm INT MSK	A/D Over-Threshold Alarm INT MSK	Output #4 Fault INT MSK	Output #3 Fault INT MSK	Output #2 Fault INT MSK	Output #1 Fault INT MSK	Reserved
Interrupt Status (INT)	02	Read-Only	Over-Current INT	Over-Temp INT	A/D Over-Threshold INT	Output #4 Fault INT	Output #3 Fault INT	Output #2 Fault INT	Output #1 Fault INT	Watchdog Time-out INT
PGOOD (PGD) Voltage Masks	03	R/W	Reserved	Reserved	Reserved	Output #4 PGD Mask	Output #3 PGD Mask	Output #2 PGD Mask	Output #1 PGD Mask	Reserved
Watchdog Enable, Mask, Service	04	R/W	Reserved	Reserved	Reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	Reserved	Reserved	Reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Time-out elapsed
Device Control and I/O Status	06	R/W	Reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	Reserved	Reserved	GPOP	GPIP
Watchdog Time-out	07	R/W	WDOG time-out counter (8 bits, in 125ms increments)							
A/D Voltage Read	08	Read-Only	ADCIN pin input voltage measurement (8 bits)							
A/D Alarm Threshold	09	R/W	Alarm Threshold for ADCIN (8 bits)							
PD Status & System Clock Control	0A	R/W	Reserved	LDET	AT_DET (AS1854 only)	CLIM (not valid in Local Power mode)	PWM Clock Modulate Enable	PWM Clock Modulate Type	PWM Clock Modulation Amount D1, D0	
PD Voltage Read	0B	Read-Only	PD input voltage measurement (Valid during both PoE and Local Power operation modes)							
PD Current Read	0C	Read-Only	Reserved	Reserved	Reserved	PD input current measurement (PoE only, does not measure Local Power current)				
PD Over Current Alarm Threshold	0D	R/W	Reserved	Reserved	Reserved	PD over-current alarm trip threshold				
Outputs 1,2 Disable and Margin Control	0E	R/W	Output #2 Disable Control	Output #2 Voltage Margin setting (D6, D5, D4)			Reserved	Output #1 Voltage Margin setting (D2, D1, D0)		
Outputs 3,4 Disable and Margin Control	0F	R/W	Output #4 Disable Control	Output #4 Voltage Margin setting (D6, D5, D4)			Output #3 Disable Control	Output #3 Voltage Margin setting (D2, D1, D0)		

GPIO

The AS1854 allows the user to send basic digital information across the isolation interface using the GPIO (General-Purpose I/O). The primary and secondary sides both have a general purpose input and output pin which can be used to send user-specific digital information across the isolation interface.

POWER OUTPUTS

The AS1854 has four power outputs which can be configured to process a total of 25.5W of input power over a range of voltages (AS1834 is limited to 13W). The AS1854 User's Guide is not intended to describe the analog configuration and behavior of these outputs. The configuration and operation of the power outputs is described in detail in the AS1854 Design Guide and AS1854 Datasheet.

The four power outputs can be individually controlled and adjusted via the I^2C interface. Gross adjustment is done externally via resistors and cannot be performed using the I^2C interface. However, each output may be margined using the I^2C interface.

ADC

The AS1854 contains an ADC (Analog-to-Digital Converter) which provides the digitally encoded information on the absolute voltage being supplied by the PSE, as well as the voltage on the dedicated input pin, ADCIN. The ADCIN input can also be used for a user-specific analog measurement (e.g. temperature)

For the PSE voltage, the ADC provides a digital range of 0V to 60V in ~0.236V increments. The PSE ADC minimum update rate is approximately 100Hz.

For the dedicated ADCIN input, the ADC will provide a digital range of 0V to 2.55V in ~0.100V increments, with the same 100Hz update rate. AS1854 also supports a comparator to detect when the ADCIN voltage value crosses a threshold. Status and/or an interrupt can be generated for this event.
See section "ADC/IADC" on page 15 for a detailed description of the register interface and encoding scheme.

IADC

The AS1854 contains a 5-bit IADC output which measures the current (I) being supplied by the PSE. The IADC does not operate in local-power mode. The digital range is 0mA to 400mA in 12.9mA increments or 0mA to 800mA in 25.8mA increments. The IADC update rate is approximately 100Hz.

WATCHDOG TIMER

The AS1854 contains a programmable watchdog timer. This timer is programmable via a register. The 8-bit timeout value can be set from 0.125s to 31.875 seconds in 0.125s increments. Timeout behavior is also programmable. It can be programmed to generate a hardware interrupt or a power-good fault. It is fully controllable via the I^2C registers. See "Watchdog Timer Operation" on page 11 for details on how to program this feature.

INTERRUPT CONTROLLER

The AS1854 can be programmed to generate an interrupt (via the INTB pin or PGOOD pin) for many different events. Each interrupt event is individually and globally maskable. The possible interrupt events

are:

- Watchdog Timer Timeout
- Over-current Alarm
- Over-temperature Alarm
- Over ADCIN Threshold Alarm
- Power-Good Fault On Any Power Output

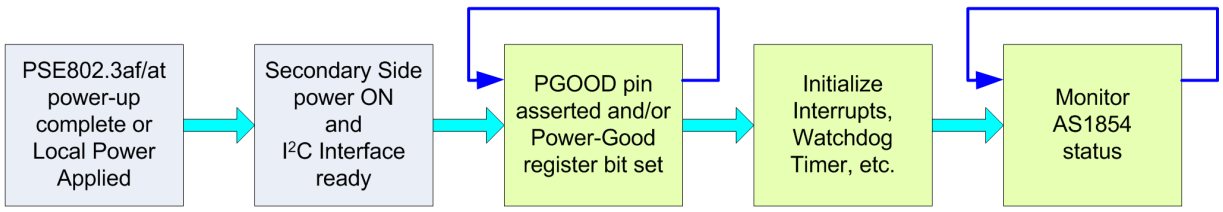
INITIALIZATION AND RESET

This section describes the power-up and initialization steps required.

POWER-UP

The diagram below describes the power-up sequence as seen by the user and should be used to help determine when power-up is complete and the system is stable.

Figure 5 - Power-Up Sequence



The AS1854 is defined as stable when all enabled power outputs are powered up and stable. This is indicated by the PGOOD pin being asserted high as well as bit 0 of register 0x00 being set to 0. One possible application of the PGOOD pin is as an active-low reset pin into the I^2C master. This guarantees that the I^2C master will not generate any transactions to the AS1854 until it is guaranteed to be stable and ready to receive transactions.

In a system where the PGOOD pin is not used to hold the I^2C master in reset, the I^2C master must poll the registers by writing a known value and reading back to determine when the registers come out of reset. A R/W register such as 0x09 (ADCIN Alarm Threshold) can be used for this purpose. All registers will be held in reset and read back as 0 until the Global PGOOD Fault has cleared.

RESET

A software reset can be performed to the secondary-side registers via bit6 of register 0x06. This will reset the value of most registers back to their Reset value (as defined in Table 2). Note: Registers 0x04 and 0x05 are NOT reset by a software reset. However, while a software reset condition is active, all registers will read back as 0, even if their values are not actually reset by the condition.

A software reset condition can also be caused by a Global PGOOD fault unless the PGOOD Reset Disable bit (bit 4 of register 0x06) is set.

PROGRAMMING

Once power-up and initialization is complete, the I^2C interface can be used to set various programmable features such as interrupts, thresholds, and timeouts.

PROGRAMMABLE INTERRUPTS

The AS1854 can be programmed to allow certain events to generate a hardware interrupt to an external controller. Register 0x01 contains the interrupt mask controls for everything except the watchdog interrupt mask which is register 0x04. Setting any mask bit to a 0 in these registers disables interrupt generation for the corresponding condition. All interrupts are disabled at reset. The table below shows all the bits related to interrupt control. Bits not related are grayed out for clarity.

Table 3 - Registers Containing Interrupt Control Bits

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
Interrupt Mask (INT MSK)	01	R/W	Over-Current Alarm INT MSK	Over-Temp Alarm INT MSK	A/D Over-Threshold Alarm INT MSK	Output #4 Fault INT MSK	Output #3 Fault INT MSK	Output #2 Fault INT MSK	Output #1 Fault INT MSK	Reserved
Interrupt Status (INT)	02	Read-Only	Over-Current INT	Over-Temp INT	A/D Over-Threshold INT	Output #4 Fault INT	Output #3 Fault INT	Output #2 Fault INT	Output #1 Fault INT	Watchdog Time-out INT
PGOOD (PGD) Voltage Masks	03	R/W	Reserved	Reserved	Reserved	Output #4 PGD Mask	Output #3 PGD Mask	Output #2 PGD Mask	Output #1 PGD Mask	Reserved
Watchdog Enable, Mask, Service	04	R/W	Reserved	Reserved	Reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	Reserved	Reserved	Reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Time-out elapsed
Device Control and I/O Status	06	R/W	Reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	Reserved	Reserved	GPOP	GPIP

In addition, the global interrupt enable (bit 5 register 0x06) must also be set to allow interrupt generation. When an interrupt is generated, the corresponding bit in register 0x02 is set high, and the INTB pin is driven low (the INTB pin is open-drain and is driven low on assertion). If this global enable is not set, then no new interrupts can be generated, but unserviced interrupts still retain their status.

The interrupt service routine can read the interrupt status register to determine the cause of the interrupt. By reading the status register, all interrupt conditions are cleared, and the INTB pin is de-asserted. Register 0x00 will always display the current status of the related condition even when the interrupt mask is 0 for that condition.

POWER-GOOD FAULT SETTINGS (PGOOD GENERATION)

Each of the four power outputs has an individual power-good fault indicator located in bits [4:1] of register 0x00, and a power-good fault history indicator located in bits [4:1] of register 0x05. PGOOD fault conditions are caused by an over-voltage, under-voltage condition, or a short-circuit condition on a specific power output that lasts for at least 10 µs. During a power-good fault, the bits in both registers 0x05 and 0x00 are set; after the fault clears (which requires 10 µs of good operation), the bit in register 0x00 clears but the bit in register 0x05 retains its set value in order to indicate that a power-good fault occurred at some point in the past. The values in register 0x05 can only be cleared by writing a 0 to the desired location. Writing a 1 has no effect and will be ignored. If the fault bit is cleared but the power-fault condition has not resolved itself, then the power-good fault history bit will be set again. The table below shows registers bits related to PGOOD generation (bits not related are grayed out for clarity).

Table 4 - Registers with Bits Related to Power-Good

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
PGOOD (PGD) Voltage Masks	03	R/W	Reserved	Reserved	Reserved	Output #4 PGD Mask	Output #3 PGD Mask	Output #2 PGD Mask	Output #1 PGD Mask	Reserved
PGOOD & Watchdog History	05	R/W	Reserved	Reserved	Reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Time-out elapsed
Device Control and I/O Status	06	R/W	Reserved	Reset all registers	Enable Interrupts	Disable PGOOD reset	Reserved	Reserved	GPOP	GPIP

Register 0x03 can be programmed to individually mask out fault conditions from each power output. Setting a 1 for a given output will enable a Global PGOOD fault for that output. A Global PGOOD fault causes the external PGOOD pin to go low for at least 10ms. This can be used as another interrupt level if desired (e.g. a non-maskable interrupt).

In addition, a Global PGOOD fault can also be used to generate a software register reset if the Disable PGOOD reset (bit 4 of register 0x06) is not set. This reset will NOT reset registers 0x04 or 0x05. Note, in the case where a power output is externally disabled (see the AS1854 Design Guide), it is guaranteed that the PGOOD fault for that power output will never assert. Therefore, the software can set the PGOOD fault mask for all power outputs even when certain outputs are disabled.

WATCHDOG TIMER OPERATION

The watchdog timer can be configured (via hardware) to automatically start at power-up or be disabled by default. This is done by either floating the WDOG_MODE pin (auto-start) or pulling the WDOG_MODE pin high (disabled pending software start). The watchdog timer can also be disabled completely by pulling WDOG_MODE low. If configured for auto-start, the watchdog timer will timeout after approximately 32 seconds after the AS1854 reaches a stable "power-good" state.

If disabled by default, the watchdog timer must be enabled explicitly via the I^2C interface. Enabling the Watchdog Timer requires two consecutive I^2C operations: Setting Watchdog Enable (bit 4 register 0x04) along with the desired value of Watchdog Interrupt Mask, Watchdog PGOOD Mask and Watchdog

Register Reset Mask bits, followed by a consecutive write to register 0x00 with the pattern 0xBB. Bits [4:1] of register 0x04 cannot be set any other way, and cannot be changed (they are read-only) when Watchdog Enable is high, and do not change during a software reset. Note: This means that they can only be written to once after power up and cannot be modified after that. The values of bits [4:1] will not actually be set until the write of 0xBB to register 0x00 is completed.

Bits [3:1] of register 0x04 are use to set the behavior of the AS1854 when a timeout occurs. If bit 3 is set to 1, then an interrupt will be generated. If bit 2 is set a 1, then a timeout is treated like a Power-Good fault event and PGOOD will be pulled low (see Table 5). Finally if bit 1 is set to a 1, then the watchdog timeout will not cause a software reset of the register space.

In addition to the timeout behavior described above, the watchdog timer will normally reload to its start value and begin counting down again immediately. However, if the Watchdog Register Reset Mask (bit 1 of register 0x04) is not set, then the timer start value will be reset to 31.875 seconds instead.

To reset or service the watchdog timer prior to timeout, the Watchdog Service Control bit (bit 0, register 0) can be used. Servicing the Watchdog function via software requires two consecutive I^2C operations: First, a write to this register, setting the Service Watchdog bit, followed by a consecutive write to register 0x00 with the pattern 0xAA. The write to 0x00 must occur prior to the next timer timeout. Even at the minimum timeout period of 125ms, there should be ample time to perform two writes on the I^2C interface at 400KHz. Note that since register 0x00 is read-only, these extra writes will not alter the contents of the register.

Table 5 - Watchdog Timer

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Watchdog Enable, Mask, Service	04	R/W	Reserved	Reserved	Reserved	Watchdog Enable	Watchdog Interrupt Mask	Watchdog PGOOD Mask	Watchdog Register Reset Mask	Watchdog Service Control
PGOOD & Watchdog History	05	R/W	Reserved	Reserved	Reserved	Output #4 caused PGOOD fault	Output #3 caused PGOOD fault	Output #2 caused PGOOD fault	Output #1 caused PGOOD fault	Watchdog Time-out elapsed
Watchdog Timeout	07	R/W	WDOG time-out counter (8 bits, in 125ms increments)							

The timer duration is set in register 0x07. This is an 8-bit linear encoding in 125ms increments. The value 0x00 is reserved and should not be used. The value written to this register will take effect at the next watchdog timer timeout or watchdog servicing event.

For example:

- 0x01 = 125ms
- 0xFF = 31.875s

Example Watchdog Programming

1-second Timeout w/ Interrupt:

```
Write 0x07 => 0x07          ; 1 Second Timeout Value
Write 0x06 => 0b001x00xx    ; Ensure Interrupts Are Enabled
Write 0x04 => 0b00011010    ; Enable timer w/Interrupt, No PGOOD Fault, No Reg. Reset
Write 0x00 => 0xBB          ; Enable Timer
```

Service Routine To Reset Counter and load new timeout value to 10seconds:

```
Write 0x07 => 0x01001111    ; 10-second timer value
Write 0x04 => 0b000xxxx1    ; Set Service Bit
Write 0x00 => 0xAA          ; Reset Counter
```

OUTPUT DISABLING AND MARGINING CAPABILITY

All four power outputs have individual voltage-margining capability for doing small adjustments to the voltage reference. These margin adjustments are located in bits [6:4], [2:0] of registers 0x0E and 0x0F. These 3-bit fields represent a +6% to -8% adjustment to voltage reference in 2% increments. This applies to all four of the margining fields. Another way of describing the encoding is as a 3-bit, 2's-complement value multiplied by 2%.

Once enabled in hardware, Power Outputs #2 thru #4 can be independently enabled or disabled in both Hardware (via pin control) and Software (via I²C register). Each output has an independent enable pin (EN2, EN3, EN4) for hardware enabling, and, can also be used to delay one voltage output relative to other. Note that Output #1, the main device power output, is always enabled and does not have an output enable pin or software control mode. Any power output to be software controlled (#2-#4) must first have been enabled in hardware. The ENx pins have internal pull-ups so outputs are power-on enabled when the ENx pins float. For Software control of Outputs #2-#4, see the output disable control bit maps in Register 0E(h) and Register 0F(h).

Table 6 - Margin Control

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Outputs 1,2 Disable and Margin Control	0E	R/W	Output #2 Disable Control	Output #2 Voltage Margin setting (D6, D5, D4)			Reserved	Output #1 Voltage Margin setting (D2, D1, D0)		
Outputs 3,4 Disable and Margin Control	0F	R/W	Output #4 Disable Control	Output #4 Voltage Margin setting (D6, D5, D4)			Output #3 Disable Control	Output #3 Voltage Margin setting (D2, D1, D0)		

Table 7 - 3-bit Voltage Reference Adjustment Encoding

Bits	Voltage Adjust
000	0% (default)
001	2%
010	4%
011	6%
100	-8%
101	-6%
110	-4%
111	-2%

SETTING LIMITS AND ALARMS

The user can set specific threshold values for voltage and current values which generate alarms and interrupts. Registers 0x09 and 0x0D can be programmed with threshold values. When the measured value is greater than the threshold for more than 10ms, the alarm bit in register 0x00 is set and if the interrupt is not masked, an interrupt is generated. See section "ADC/IADC" on page 15 for details on the encoding of the ADC and IADC values and thresholds.

Table 8 - Alarms

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Alarms and Power Status	00	Read-Only	Over-Current Alarm	Over-Temp Alarm	A/D Over-Threshold Alarm	Output #4 Fault	Output #3 Fault	Output #2 Fault	Output #1 Fault	Global PGOOD Fault
Interrupt Mask (INT MSK)	01	R/W	Over-Current Alarm INT MSK	Over-Temp Alarm INT MSK	A/D Over-Threshold Alarm INT MSK	Output #4 Fault INT MSK	Output #3 Fault INT MSK	Output #2 Fault INT MSK	Output #1 Fault INT MSK	Reserved
Interrupt Status (INT)	02	Read-Only	Over-Current INT	Over-Temp INT	A/D Over-Threshold INT	Output #4 Fault INT	Output #3 Fault INT	Output #2 Fault INT	Output #1 Fault INT	Watchdog Time-out INT

In addition to ADC-In voltage and PSE current, the AS1854 also monitors temperature. The "Over-Temp Alarm" (bit 6, register 0x00) is set when the junction temperature measured at the PD controller exceeds 145°C. If the junction temperature reaches 160°C, the AS1854 will shutdown. As with the voltage and current alarms, an interrupt will be generated unless masked.

MONITORING AND STATUS

Once the AS1854 has been configured for interrupts, thresholds and timeouts, the external controller should be able to go into a normal monitoring loop polling values (if desired) and waiting for any interrupts. The watchdog timer and its associated interrupt can be used as a way to periodically poll specific values such as ADC and IADC values as well as miscellaneous status information.

ADC/IADC

The PSE voltage and current can be monitored by reading registers 0x0B and 0x0C.

Table 9 - ADC/IADC Registers

Register	Addr (hex)	Access	Data Bits							
			D7	D6	D5	D4	D3	D2	D1	D0
A/D Voltage Read	08	Read-Only	ADCIN pin input voltage measurement (8 bits)							
PD Status & System Clock Control	0A	R/W	Reserved	LDET	AT_DET (AS1854 only)	CLIM (Note that CLIM status is not valid in Local Power mode (LDET status bit D6=1)).	PWM Clock Modulate Enable	PWM Clock Modulate Type	PWM Clock Modulation Amount D1, D0	
PD Voltage Read	0B	Read-Only	PD input voltage measurement (Valid during both PoE and Local Power operation modes)							
PD Current Read	0C	Read-Only	Reserved	Reserved	Reserved	PD input current measurement (PoE only, does not measure Local Power current)				

The PoE voltage value read from register 0x0B is linearly encoded in approximately 0.236V increments. A value of 0x00 is 0V and a value of 0xFF is a value of 60V (maximum allowed voltage by PSE). In a failure situation where the PSE provided more than 60V to the AS1854, the ADC value will remain saturated at 0xFF.

The PoE current value read from register 0x0C is linearly encoded. The value of this field depends on the PoE Current Limit bit (bit 4, register 0x0A). If this bit is 1, then the PoE current range is from 0mA to 800mA. If this bit is 0, then the range is 0mA to 400mA. With PoE Current Limit=800mA, 0x00=0mA, 0x1F=800mA and the increments are 25.8mA each. Likewise, with PoE Current Limit=400mA, 0x1F=400mA and the increments are 12.9mA each.

It is recommended that the value read from the PSE Current register be averaged over time due to instantaneous changes and surges in current.

The ADC-In (user ADC) value can be monitored via the 0x08 register. This register value represents a linear-encoding voltage on the ADCIN pin between 0V (0x00) and 2.5V (0xFF) in approximately 0.100V increments. If the voltage on the ADCIN pin exceeds 2.5V, the ADC will saturate at 0xFF.

All ADC and IADC register fields have an update rate of 100Hz (10ms period). The ADC and IADC

subsystems on the primary side actually have an update rate of 1.5KHz, but the information is only transmitted at a 100Hz update rate.

MISCELLANEOUS STATUS BITS

There are a number of miscellaneous status bits which report the current operating state of the PD controller:

Bit 6 of register 0x0A indicates the presence of local power. A value of 1 on this bit indicates that local power is connected. PSE may also be connected, but power is being supplied by local power in this case. Under local power, certain functions no longer operate. The PSE Current value in register 0x0C is no longer valid and is set to 0x00. The meaning of Bit 5 in register 0x0A also is changed. The PSE, if connected, may NOT be an 802.3at-capable supply, but because the AS1854 is connected to a local supply, it can supply more power.

Bit 5 of register 0x0A is the 802.3at detection bit. If this bit is set it means that either the PSE has indicated it is 802.3at capable (can supply up to 30W of power), or the AS1854 is connected to local power, which is indicated on bit 6 of register 0x0A.

Bit 4 indicates the current-limit configuration of the PD controller and how to interpret the value present for PoE current in register 0x0C. See section "ADC/IADC" on page 15 for more details on the PoE current measurements in register 0x0C.

GPIO SETTING AND POLLING

In software mode, there are no external GPIO pins on the secondary side. Setting GPOP and sensing the GPIP on the primary side is done via register reads and writing to bits [1:0] of register 0x06. To set the value present on the GPOP pin on the primary side, the value is written to bit 1 of register 0x06. The value present on the GPIP pin on the primary side can be read from bit 0 of register 0x06.

EXAMPLE PSEUDO CODE

This section contains example pseudo code for initialization, programming, monitoring and servicing the AS1854. It is provided to clarify usage models, and is not intended to be considered the only way that software control can be implemented.

The example below is for a video camera with external light sensor and external light.

PSEUDO CODE CONVENTIONS

The following instruction words are used:

```
write <reg>, <data>           Write <data> (via I2C) to AS1854 register <reg>
$a=read <reg>                 Read data from AS1854 register (via I2C) and
store in symbol $a
//<comment>             Comment text
```

INITIALIZATION AND CONFIGURATION CODE

```
initialize()
      {
      //wait for power-good
      $a=0;
      while($a != 0x55)
         {
         write 0x09, 0x55; // use alarm threshold register to poll for pgood
         $a=read 0x09;
         }

      ////////////////////////////
      //CHECK OPERATING CONDITIONS
      ////////////////////////////
      $pd_status=read 0x0A;
      $local_power=$pd_status &0x40;
      $at_mode=$pd_status & 0x20;
      $current_limit=$pd_status & 0x10;

      ////////////////////////////////////////////////
      //SETUP LIMITS and ALARMS                     //
      ////////////////////////////////////////////////
      //ADCIN being used for external light sensor
      //when value is > about 128, light is too low, to turn on ext.light
      write 0x09,0x80;

      //set IADC threshold at about 90% of max (90% of 0x1F = 0x1B)
      write 0x0D, 0x1B;

      ////////////////////////////////////////////////
      //SETUP INTERRUPTS
      ////////////////////////////////////////////////
      //First, make sure interrupt status is cleared
      $int_status=read 0x02; //read clears status
      //Now enable interrupts for over current, over temp and ADCIN threshold
      write 0x01, 0b11100000;
```

```
      //Do not turn on INTB pin yet, wait until done with all setup

      ////////////////////////////////////////////////
      //SETUP HIGH-PRIORITY INTERRUPT (PGOOD)
      ////////////////////////////////////////////////
      write 0x03, 0b00011110;  //Enable all 4 power-output fault indicators
      write 0x06, 0b00010000;  //Disable reset on PGOOD,reset handled by sw

      ////////////////////////////////////////////////
      //SETUP WATCH DOG
      ////////////////////////////////////////////////
      //Enable timer and enable for interrupts, no reset of registers
      write 0x04,0b00011010;
      write 0x00,0xBB; //special write required for enable wdog
      //watchdog timer now running with default 32-second timer


      //Set timer value to 1 second
      write 0x07,0x08;  //1-second timeout
      //After Next Timeout timer will start 1-second timeout

      ////////////////////////////////////////////////////////
      //ENABLE INTERRUPTS
      ////////////////////////////////////////////////////////
      $dev_ctrl=read 0x06;
      $dev_ctrl |= 0b00100000;
      write 0x06, $dev_ctrl;
      //interrupts now enabled
}

int_handler_routine()
   {
   // temporarily disable interrupts
   $dev_ctrl=read 0x06;
   $dev_ctrl &= 0b11011111;
   write 0x06, $dev_ctrl;

   // read interrupts status and clear interrupts
   $int_status=read 0x02;
   $over_current=$int_status & 0x80;
   $over_temp=$int_status & 0x40;
   $over_adcin_thresh=$int_status & 0x20;
   $time_out=read 0x05 & 0x01;

   //not using pgood fault INT, not enabled
   $pgood_fault = $int_status & 0x01;

   if($over_temp)
       {
       call severe_error_handler("Power System Failure: Temperature Too
High\n");
       call shutdown();
       }
   if($over_current)
      {
      call warning_handler("Power System Warning: Reaching Maximum Power
Levels\n");
```

```
      //Disable interrupt and switch to active monitoring
      $monitor_current=1;
      $int_mask=read 0x01;
      $int_mask&=0x7F;  //Disable interrupt for over current
      }
   if($over_adcin_thresh)
      {
      $ext_light=1;
      //Disable interrupt for ADCIN (light level)
      $monitor_light=1;
      $int_mask=read 0x01;
      $int_mask&=0xDF;  //Disable interrupt for ADCIN threshold
      call ext_light_control($ext_light);
      }
    if($time_out)
       {
       $local_power=(read 0x0A) & 0x80;
       $pse_current=read 0x0C & 0x1F;
       $adc_in=read 0x08;
       call monitor_routine ($monitor_current, $monitor_light, $local_power,
$pse_current, $adc_in);
       }

   // re-enable interrupts
   $dev_ctrl |= 0b00100000;
   write 0x06, $dev_ctrl;

   }

hi_pri_int_handler_routine()
   {
   //This routine handles PGOOD de-assertions like a high-priority interrupt
   $pgood_status=(read 0x05) &0x01;
   if($pgood_status)
      {
      call severe_error_handler("Power System Failure: Power Delivery Fault
Detected\n");
      call shutdown();
      }
   }


ext_light_control($ext_light)
   {
   //This routine controls an external light via the general-purpose IO
   //set GPOUT to turnon external light
   $dev_ctrl=read 0x06;
   $dev_ctrl|=0x02;
   write 0x06, $dev_ctrl;
   $light_on=0;
   //wait for light to actually turn on;
   //check GPIN
   while(! $light_on)
      {
      $light_on=(read 0x06&0x01);
      }
   }
```

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