High Efficiency 8-CH LED Backlight Driver with Dual LCD Bias Power

Features

- Backlight LED Driver
  - Wide input range: 2.7V~5.5V
  - High efficiency step-up LED driver with 8-Ch current sinks, up to 40V boost voltage.
    - Up to 30mA/Ch in backlight mode
    - ±0.7% current matching at 20mA
    - ±2.2% current accuracy at 20mA
  - I^2C/PWM dual dimming control scheme
    - High resolution I^2C 11-bit linear or exponential dimming
    - Wide range PWM dimming.
      - 100Hz to 100kHz frequency
      - 0.2% to 100% duty cycle at 20kHz
  - Programmable current sink turn on/off ramp time/shape and transition ramp up/down time.
  - 1.0MHz typical boost switching frequency
  - Programmable input PWM hysteresis to minimize jitter at low PWM duty cycle.
  - Programmable OVP and current limit
  - LED open/short protection
- LCD Panel Bias
  - Wide input range: 2.7V~5.5V
  - Programmable dual output Bias regulator using a single inductor.
  - Programmable ramp time for OUTP and OUTN
  - Charge pump PFM mode at light load
  - LCD Bias efficiency: up to 85%
  - Wide dual output voltage range ±4.0V to ±6.3V (50mV/step) and output current up to 250mA at $V_{IN} \geq 2.9$ V.
  - Active output discharge function
  - Current limit and short protection
- Others
  - System level input UVLO
  - Thermal shutdown protection
  - Low shutdown current <1μA
  - Flexible I^2C interface
  - Pb-free Packages:
  - WQFN55-32 (5mm x 5mm, 32 Lead)
  - RoHS and Green Compliant
  - -40°C to +85°C Temperature Range

Brief Description

KTZ8868 is the ideal power solution for LED backlighting and LCD bias power of medium size panels. It integrates two step-up converters for LED backlighting, a step-up converter with LDO and inverting charge pump for LCD bias power, resulting in a simpler and smaller solution with fewer external components. High switching frequency allows the use of smaller inductors and capacitors. Its input operating range is from 2.7V to 5.5V, accommodating 1-cell lithium-ion batteries or 5V supply.

The LED driver has two step-up converters, and each converter drivers four current sinks with total eight current sinks. Each current sink can regulate up to 30mA with its maximum boost output voltage up to 40V. 11-bit linear or exponential I_{LED} resolution can be obtained over I^2C or PWM dimming. For additional flexibility, PWM dimming offers wide range frequency and duty cycle to support Content Adaptive Brightness Control (CABC).

The LCD bias power section includes a step-up converter, LDO and an inverting charge pump to generate dual outputs, OUTP and OUTN, whose voltages can be programmed via an I^2C interface. By integrating synchronous rectification MOSFETs for the step-up converter and charge pump, the KTZ8868 maximizes conversion efficiency up to 85%.

Various protection features are built into KTZ8868, including inductor current limit protection, output short circuit protection, output over-voltage protection, LED fault (open or short) protection and thermal shutdown protection.

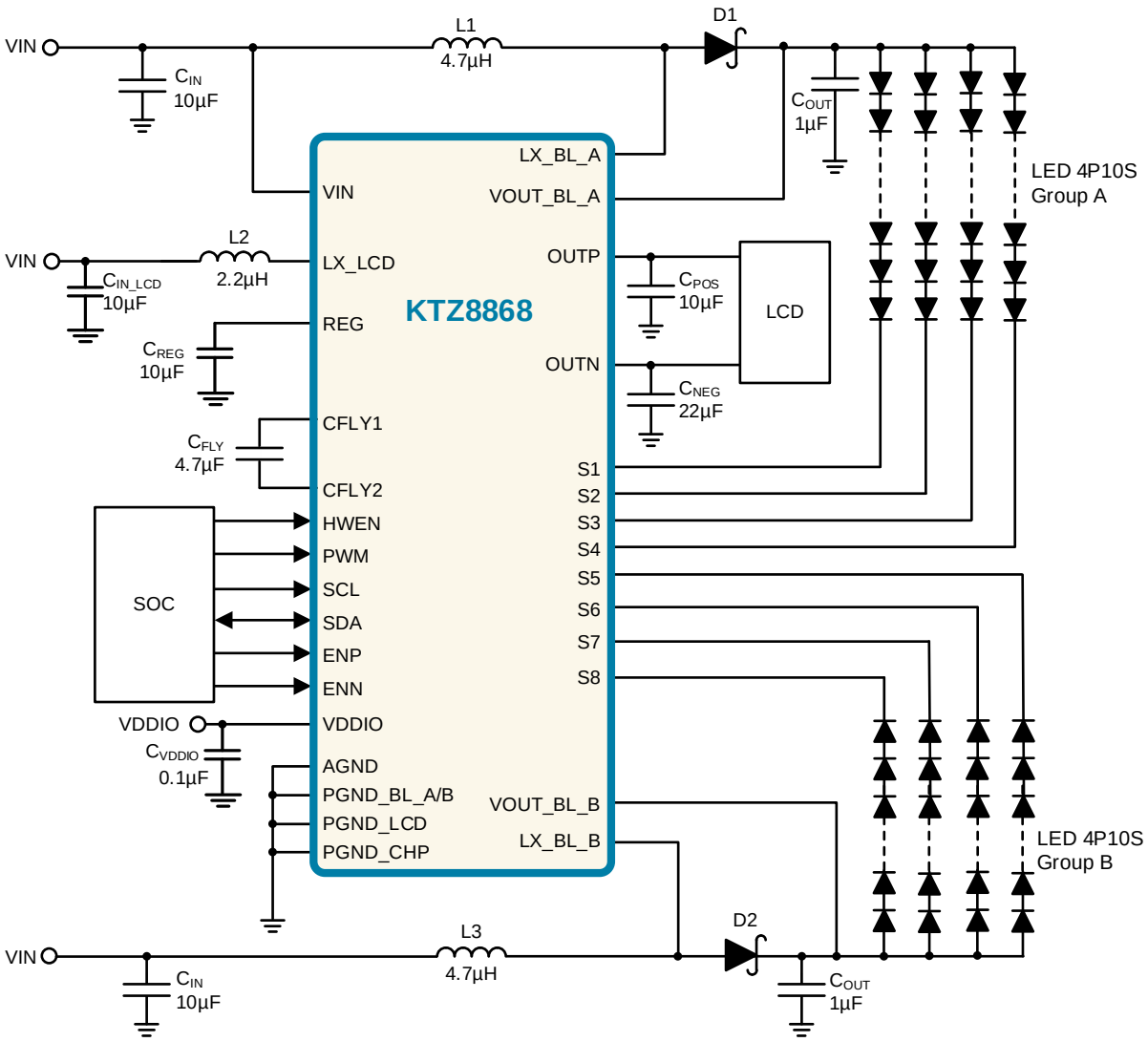
KTZ8868 is equipped with I^2C interface for various controls and status monitor.

KTZ8868 is available in a RoHS and Green compliant WQFN55-32 (5mm x 5mm, 32 Lead).

Applications

- Tablet Backlight and Bias

Typical Application

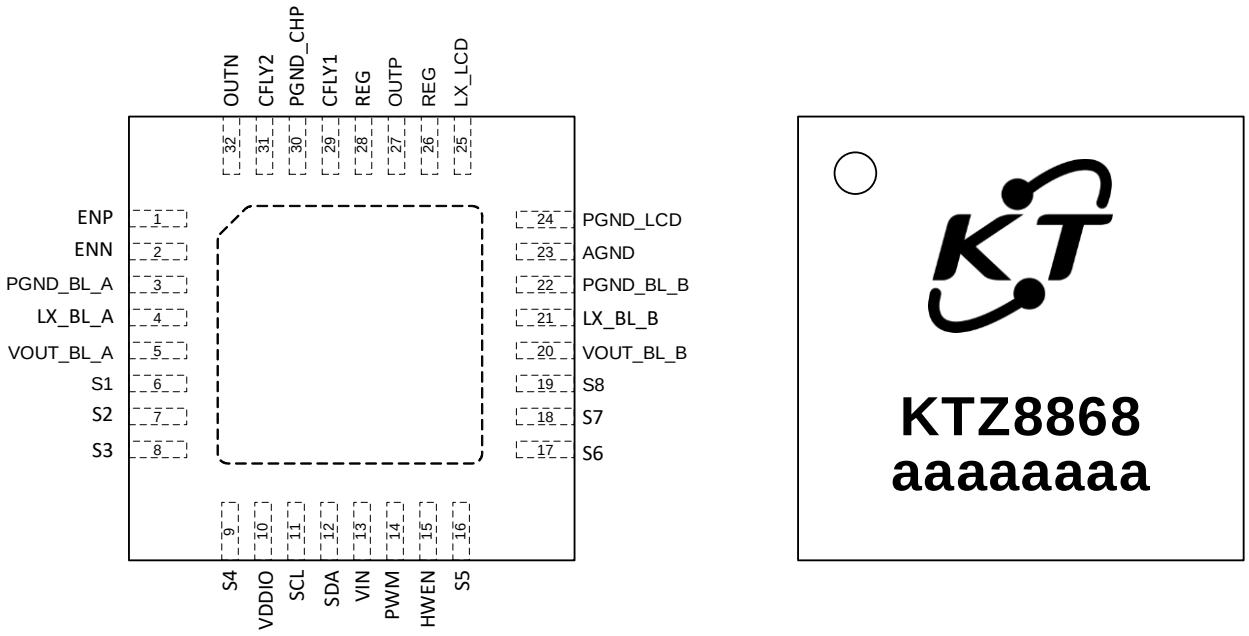


Ordering Information

Part Number	Marking[1]	Operating Temperature	Package
KTZ8868EUAD-TB	aaaaaaaa	-40°C to +85°C	WQFN55-32

Pinout Diagram

WQFN55-32



32-Pin 5.00mm x 5.00mm x 0.75mm
WQFN Package, 0.50mm pitch

Top Mark
aaaaaaaa = Assembly Lot Tracking Number

1. aaaaaaaa = Assembly Lot Tracking Number.

Pin Descriptions

Pin #	Name	Function
1	ENP	Enable pin for positive power (OUTP), 300KΩ pull down resistor to GND
2	ENN	Enable pin for negative power (OUTN), 300KΩ pull down resistor to GND
3	PGND_BL_A	Power Ground for LED boost converter A.
4	LX_BL_A	Switching pin of the LED step-up converter A.
5	VOUT_BL_A	Output voltage sense pin of the step-up converter A.
6	S1	Regulated output current sink #1.
7	S2	Regulated output current sink #2.
8	S3	Regulated output current sink #3.
9	S4	Regulated output current sink #4.
10	VDDIO	Connected to system VDDIO with 0.1µF capacitor
11	SCL	Clock of the I^2C interface.
12	SDA	Bi-directional data pin of the I^2C interface.
13	VIN	Input supply pin for the IC, bypass with a 10µF ceramic capacitor to GND.
14	PWM	PWM dimming input pin, 300kΩ pull-down resistor at this pin to GND.
15	HWEN	Active high hardware enable pin, 300kΩ pull-down resistor to GND.
16	S5	Regulated output current sink #5.
17	S6	Regulated output current sink #6.
18	S7	Regulated output current sink #7.
19	S8	Regulated output current sink #8.
20	VOUT_BL_B	Output voltage sense pin of the step-up converter B.
21	LX_BL_B	Switching pin of the LED step-up converter B.
22	PGND_BL_B	Power Ground for LED boost converter B.
23	AGND	Analog ground pin.
24	PGND_LCD	Power ground for LCD Bias power supply boost converter.
25	LX_LCD	Switching node of the LCD Bias boost converter.
26, 28	REG	LCD-Bias Boost converter output pin, bypass a 10µF ceramic capacitor to PGND_LCD.
27	OUTP	LDO output pin of the positive power, bypass with a 10µF ceramic capacitor.
29	CFLY1	Negative charge pump flying capacitor pin positive connection.
30	PGND_CHP	Power ground for negative charge pump.
31	CFLY2	Negative charge pump flying capacitor negative connection.
32	OUTN	Charge pump output pin of the negative power. Bypass with a 22µF ceramic capacitor to PGND_CHP.
	Exposed Thermal Pad	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND for proper function.

Absolute Maximum Ratings[2]

Symbol	Description	Value	Units
VIN	Input Voltage	-0.3 to 6	V
LX_BL_A, LX_BL_B	LX_BL to GND DC	-0.3 to 42	V
	LX_BL to GND AC Transient: 100ns	-1.0 to 44	V
VOUT_A, VOUT_B	LED Backlight driver output node	-0.3 to 42	V
S1, S2, S3, S4, S5, S6, S7, S8	LED Backlight driver current sink	-0.3 to 32	V
HWEN, SCL, SDA, PWM, ENP, ENN, VDDIO	Control Pins	-0.3 to VIN+0.3	V
LX_LCD, CFLY1, OUTP, REG	LCD Bias power positive voltage and switching node	-0.3 to 7	V
OUTN, CFLY2	LCD Bias power negative output voltage and switching node	-7 to 0.3	V
T_J	Junction Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C
ESD	HBM Electrical Static Discharge	2.0	kV

ESD and Surge Ratings

Symbol	Description	Value	Units
VESD	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charge device model (CDM), per JEDEC specification JESD22-C101	±500	V

Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	29.1	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	4.3	W
$\Delta P_D/\Delta T$	Derating Factor Above $T_A = 25°C$	-34.4	mW/°C

2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Electrical Characteristics[4]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of –40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 3.6V.

IC Supply

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input operating range		2.7		5.5	V
UVLO	Input under voltage lockout	Rising edge		2.45	2.65	V
$UVLO_{HYST}$	UVLO hysteresis			0.05		V
I_Q	IC standby current	HWEN = VDDIO, LCD Boost disabled, LED Boost and Current Sink disabled.		1.0	5.0	µA
I_{LCD_EN}	Bias power no load current	LED Boost and Current Sink disabled. OUTP, OUTN enabled with no load.		1.0	1.5	mA
I_{SHDN}	IC shutdown V_{IN} current	HWEN = 0, ENP = ENN = GND		1.0	3.0	µA

Boost Converter A/B for LED Backlight

Symbol	Description	Conditions	Min	Typ	Max	Units
$R_{DS(ON)}$	NMOS on-resistance	V_{IN} = 3.6V, I_{SW} = 250mA, T_A = 25°C		180	300	mΩ
I_{LIM}	Peak NMOS current limit	Reg 0x11[1:0]=00, T_A = 25°C	1.02	1.2	1.38	A
F_{SW}	Oscillator frequency	T_A = 25°C	0.9	1.0	1.1	MHz
EFF_{LEDBST}	Boost Efficiency[5]	V_{IN} = 3.6V, I_{LED} = 5mA/ch, 8P6S LEDS, Typical application circuit.		87		%
D_{MAX}	Maximum duty cycle[5]	F_{SW} = 1MHz, T_A = 25°C	91	94		%
V_{OVP}	OVP threshold	Reg 0x02[7:5]=111, default, T_A = 25°C	38.5	40	41.3	V
	OVP hysteresis			2		V

Current Sink for LED Backlight

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{SINK_ACC}	Output current accuracy	Current setting = 30mA, T_A = 25°C	-2.0		2.0	%
		Current setting = 20mA, T_A = 25°C	-2.2		2.2	%
		Current setting = 1mA, T_A = 25°C	-3.0		3.0	%
I_{SINK_MATCH}	Output current matching[6]	Current setting = 30mA, T_A = 25°C	-0.7		0.7	%
		Current setting = 20mA, T_A = 25°C	-0.7		0.7	%
		Current setting = 1mA, T_A = 25°C	-1.5		1.5	%
V_{HR}	Current sink head room voltage			0.45		V
I_{LED_MIN}	Minimum LED current per string	Linear or Exponential mapping		60		µA
I_{STEP}	LED current step size[5]	Exponential Mode		0.3		%
		Linear Mode		14.63		µA
V_{SOV}	Current sink over voltage threshold[5]			6		V
T_{FAULT}	Current sink fault delay		50	60	70	ms

(continued next page)

4. KTZ8868 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
5. Guarantee by characterization and/or simulation.
6. The current matching among channels is defined as $|I_{SINK}-I_{AVG}|_{MAX}/I_{AVG}$.

Electrical Characteristics (continued)[7]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of –40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 3.6V.

Boost Converter for LCD Power Bias

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{REG}	LCD boost output voltage range		4		6.6	V
	LCD boost output voltage step size[8]			50		mV
I_{REG_LIM}	Peak current limit	V_{IN} = 3.6V, T_A = 25°C	1.6	1.9		A
F_{SW}	Oscillator frequency	Continuous Mode, T_A = 25°C	1.8	2.0	2.2	MHz
EFF_{LCDBST}	Efficiency[8]	V_{IN} = 3.6 V, V_{REG_OUT} = 5.9 V, 6mA < I_O < 400mA, Typical application circuit		85		%
R_{ON_HS}	High side FET on resistance	V_{IN} = 3.6V, T_A = 25°C		220	280	mΩ
R_{ON_LS}	Low side FET on resistance	V_{IN} = 3.6V, T_A = 25°C		200	250	mΩ
V_{REG_PP}	LCD boost output ripple[8]	Io = 5mA and 250mA, Co = 10µF		50		mV_{PP}
D_{MAX}	Maximum duty cycle		85	90		%

OUTP-Positive Output

Symbol	Description	Conditions	Min	Typ	Max	Units
OUTP	Positive output voltage range		4.0		6.3	V
	Output voltage step size[8]			50		mV
	Output voltage accuracy	V_{OUTP} = 5.5V, no load	-1.5		+1.5	%
I_{OUTP_MAX}	Maximum output current limit	V_{IN} ≥ 9V	250			mA
I_{OUTP_LIM}	Positive output current limit	V_{IN} = 3.6V, V_{REG} = 6.0V, V_{OUTP} = 5.5V, T_A = 25°C		340		mA
V_{OUTP_LOREG}	VOUTP LDO load regulation[8]	0 ≤ Io ≤ I_{OUTP_MAX}			80	mV
V_{OUTP_DO}	VOUTP LDO dropout voltage[8]	I_{OUTP} = I_{OUTP_MAX}, V_{OUTP} = 5.5V			200	mV
T_{OUTP_SS}	Startup time	Co = 10µF, V_{OUTP} = 5.75V, VOUTP_RAMP = 2b'01		456		µs
R_{PD_OUTP}	Output pulldown resistor in shutdown		40	70	100	Ω

OUTN-Negative Output

Symbol	Description	Conditions	Min	Typ	Max	Units
OUTN	Negative output voltage range		-6.3		-4.0	V
	Output voltage step size[8]			50		mV
	Output voltage accuracy	V_{OUTN} = -5.4V, no load	-1.5		+1.5	%
I_{OUTN_MAX}	Maximum output current limit		250			mA
EFF_{CHP}	Inverting charge pump efficiency[8]	V_{REG} = 5.7V, V_{OUTN} = –5.4V, I_{OUTN} > –5mA		85		%
T_{OUTN_SS}	Startup time	Co = 10µF, V_{OUTN} = -5.75V, VOUTN_RAMP = 4b'0001		912		µs
R_{PD_OUTN}	Output pulldown resistor in shutdown			20	35	Ω

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7. KTZ8868 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
8. Guarantee by characterization and/or simulation.

Electrical Characteristics (continued)[9]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of –40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 3.6V.

PWM INPUT[10]

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{PWM_INPUT}	PWM input frequency		0.1		100	kHz
t_{MIN_ON}	Minimum pulse ON time			150		ns
t_{MIN_OFF}	Minimum pulse OFF time			150		ns
PWM_{RES}	PWM input resolution	100Hz < f_{PWM} < 10KHz		11		bit

I²C-Compatible Voltage Specifications (SCL, SDA, ENP, ENN, PWM, HWEN, VDDIO)

Symbol	Description	Conditions	Min	Typ	Max	Units
VDDIO	VDDIO input voltage range		1.0		Vin+0.3	V
V_{IL}	Input Logic Low Threshold				0.35* VDDIO	
V_{IH}	Input Logic High Threshold		0.65* VDDIO			V
V_{OL}	SDA Output Logic Low	I_{SDA} = 3mA			0.4	V
RPD_{HWEN}	Pulldown resistance on HWEN pin			300		KΩ
RPD_{PWM}	Pulldown resistance on PWM pin			300		KΩ
RPD_{ENP}	Pulldown resistance on ENP pin			300		KΩ
RPD_{ENN}	Pulldown resistance on ENN pin			300		KΩ

I²C-Compatible Timing Specifications (SCL, SDA), see Figure 1[10]

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{LOW_SCL}	SCL low clock period		1.25			µs
t_{HIGH_SCL}	SCL high clock period		0.65			µs
f_{SCL}	SCL clock frequency				400	kHz
t_{SU_DAT}	Data in setup time to SCL high		100			ns
t_{V_DAT}	Data valid time				0.9	µs
t_{HD_DAT}	Data out stable after SCL low		0			ns
t_{START}	SDA low setup time to SCL low (Start)		100			ns
t_{STOP}	SDA high hold time after SCL high (Stop)		100			ns
t_{RISE}	SDA/SCL rise time	V_{PULLUP} = 1.8V, R_{PULLUP} = 1kΩ, C_{BUS} = 100pF			300	ns
t_{FALL}	SDA/SCL fall time	V_{PULLUP} = 1.8V, R_{PULLUP} = 1kΩ, C_{BUS} = 100pF			300	ns

Thermal Shutdown[10]

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{J\text{-}TH}$	IC thermal shutdown threshold			150		°C
	IC thermal shutdown hysteresis			15		°C

9. KTZ8868 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

10. Guarantee by characterization and/or simulation.

Timing Diagrams

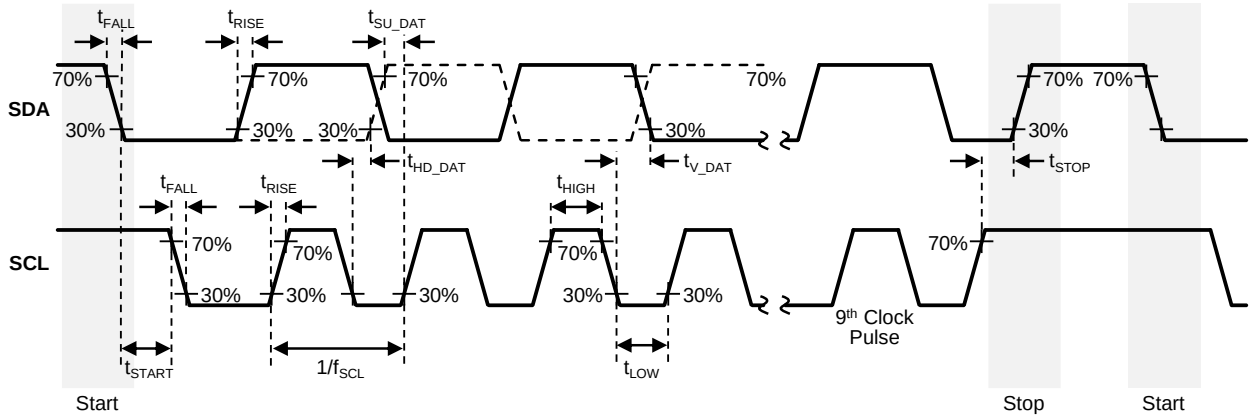


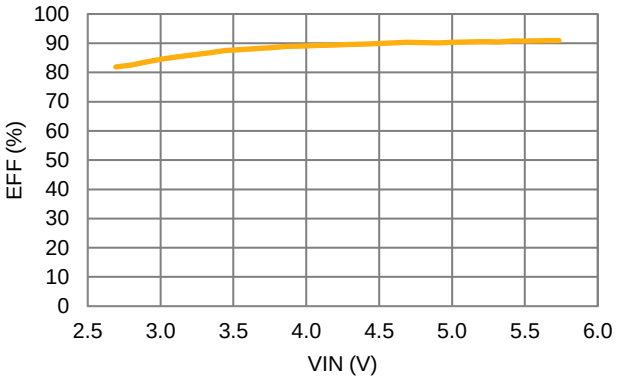
Figure 1. I²C Compatible Interface Timing

Typical Characteristics

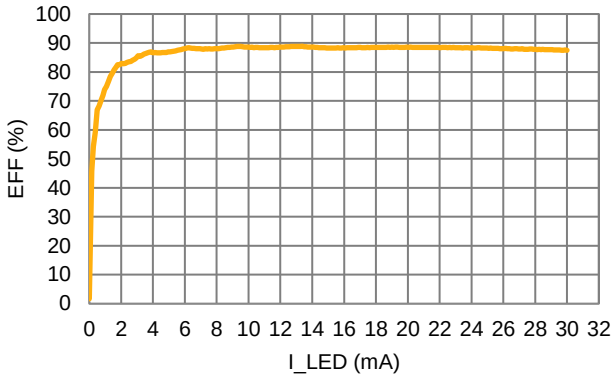
LED Backlight

V_{IN} = 3.6V, 8P6S LEDs, I_{LED} = 30mA, L = VLF504012MT-4R7M-CA, C_{IN} = 10µF, C_{OUT} = 1µF, I^2C register default settings, Temp = 25°C unless otherwise specified.

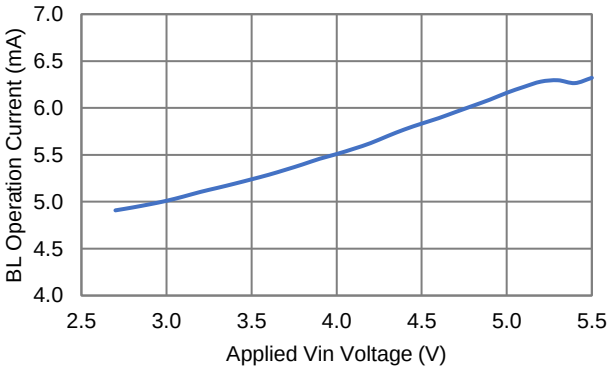
LED Driver Efficiency vs. VIN



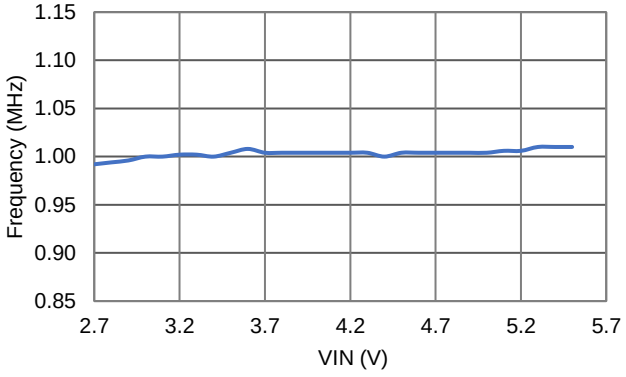
LED Driver Efficiency vs. I_LED



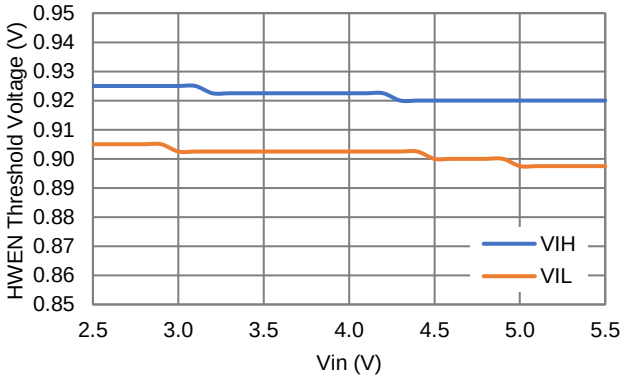
Operating Current vs. VIN



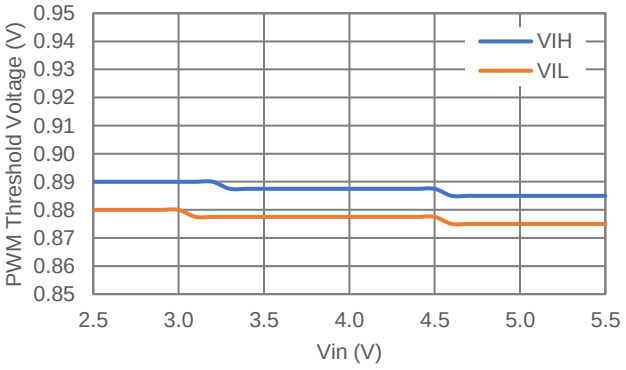
Switching Frequency vs. VIN



HWEN Logic Threshold Voltage
(Vin = 2.5V to 5.5V, VDDIO = 1.8V)



PWM Logic Threshold Voltage
(Vin = 2.5V to 5.5V, VDDIO = 1.8V)



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Typical Characteristics

LED Backlight

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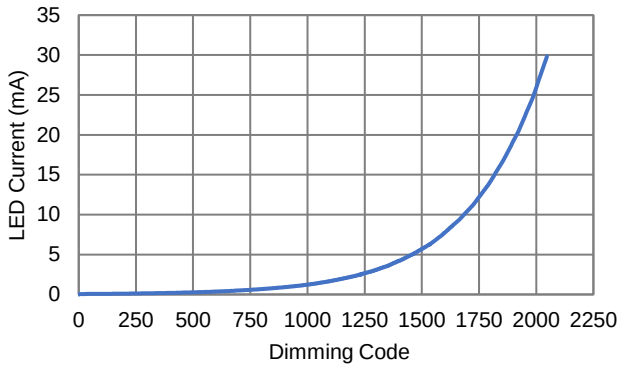
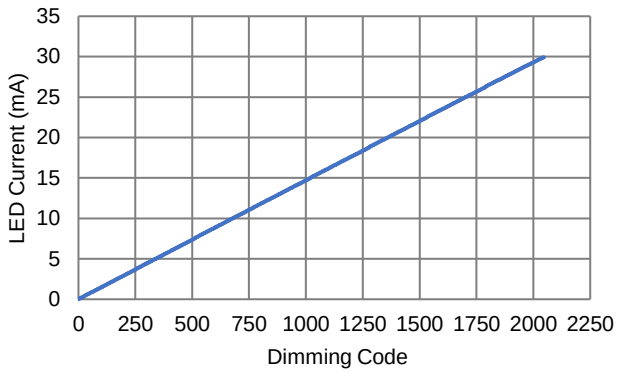
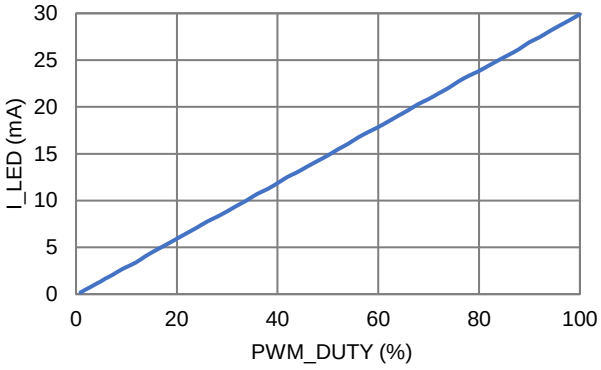
LED Current vs. Current Ratio Code
(11bits, Exponential)



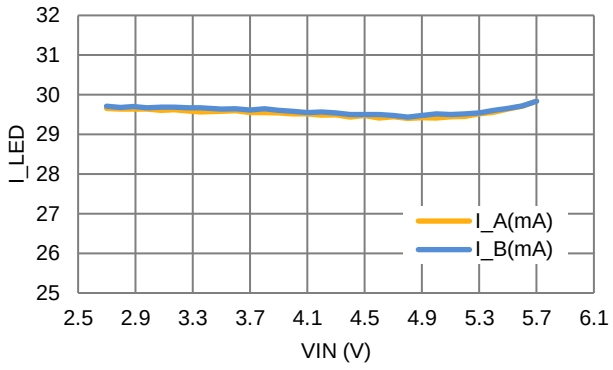
LED Current vs. Current Ratio Code
(11bits, Linear)



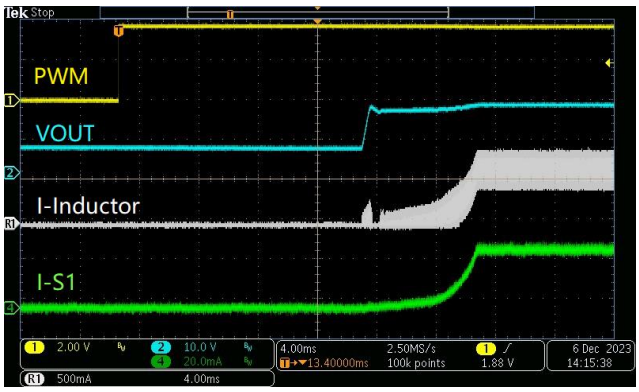
LED Current vs. PWM Duty Cycle
(20 KHz)



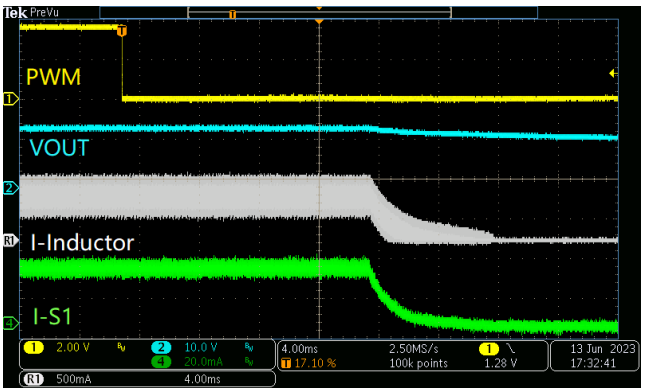
LED Current Line Regulation



Turn On by PWM
(Exponential)



Turn Off by PWM
(Exponential)



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Typical Characteristics (continued)

LED Backlight

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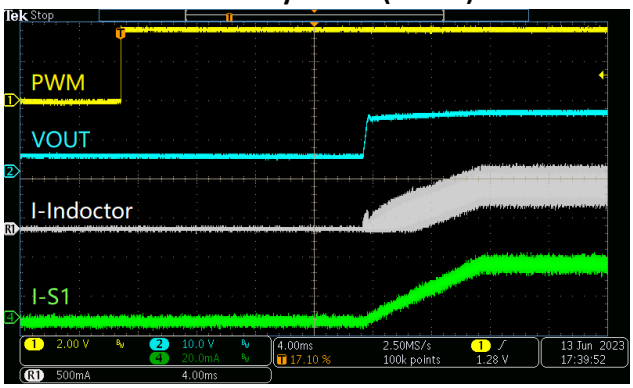
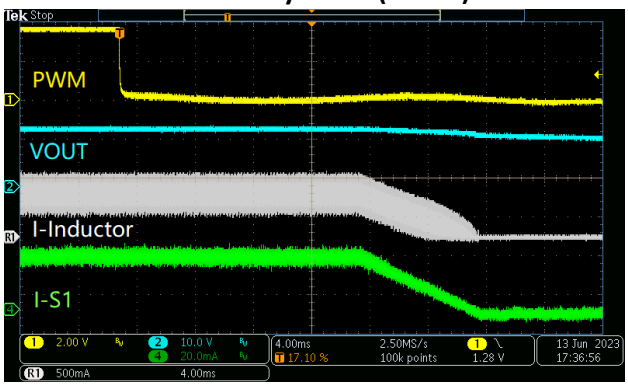
Turn On by PWM (Linear)

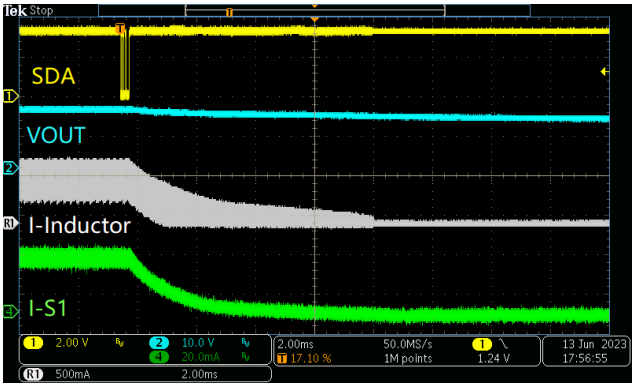


Turn Off by PWM (Linear)

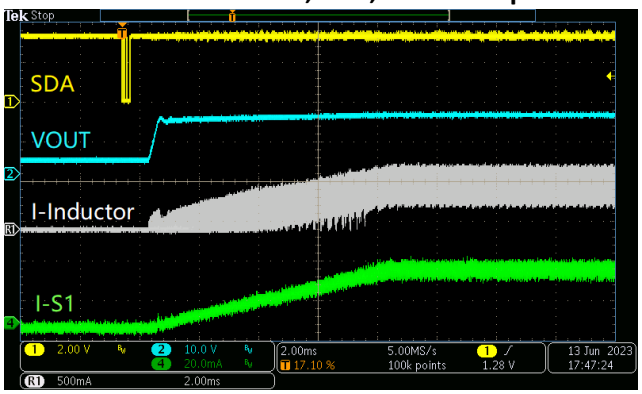


Power on via I2C, 8ms, Exponential Shape

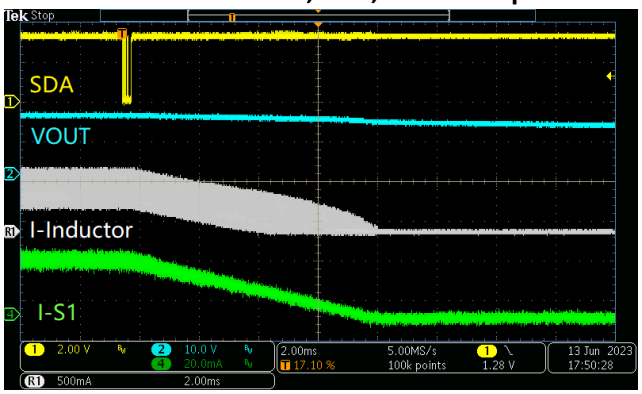
Power off via I2C, 8ms, Exponential Shape



Power on via I2C, 8ms, Linear Shape



Power off via I2C, 8ms, Linear Shape



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Typical Characteristics (continued)

LED Backlight

V_{IN} = 3.6V, 8P6S LEDs, I_{LED} = 30mA, L = VLF504012MT-4R7M-CA, C_{IN} = 10µF, C_{OUT} = 1µF, I^2C register default settings, Temp = 25°C unless otherwise specified.

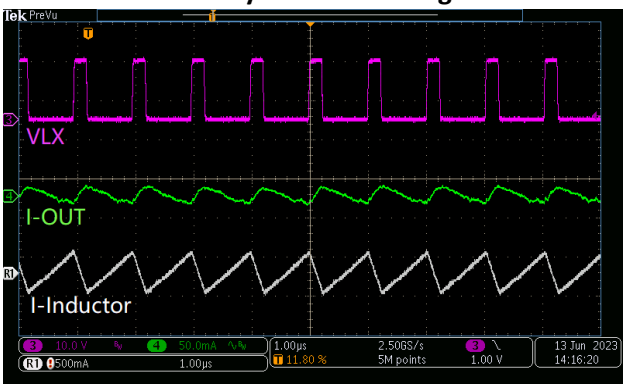
Ramp Up Waveform

I_CH from 3mA to 27mA, Linear Mapping

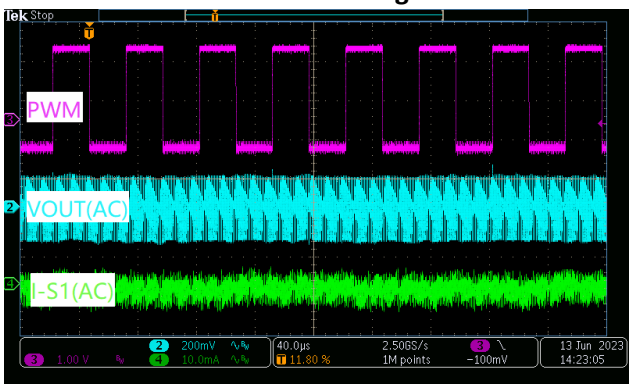
Ramp Down Waveform

I_CH from 27mA to 3mA, Linear Mapping

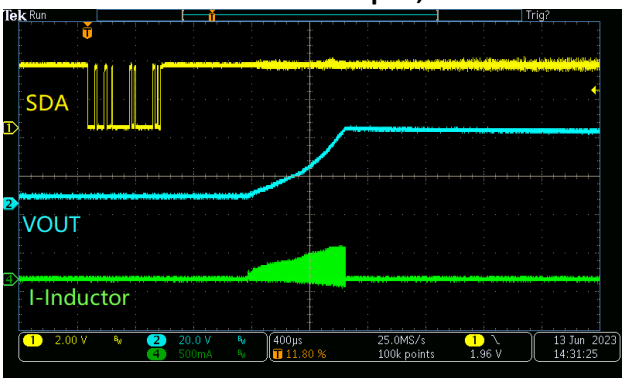
Steady State Switching



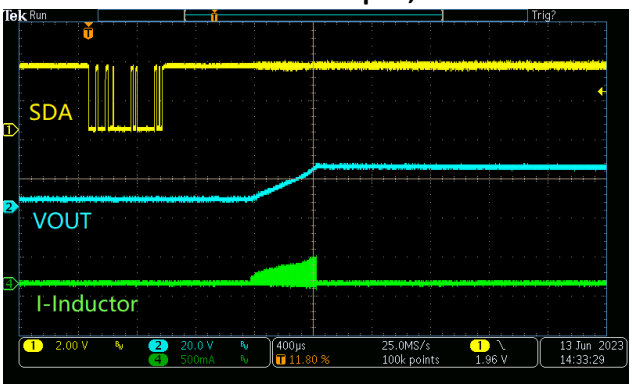
PWM Dimming



Power on with VOUT Open, 40V OVP



Power on with VOUT Open, 21.4V OVP



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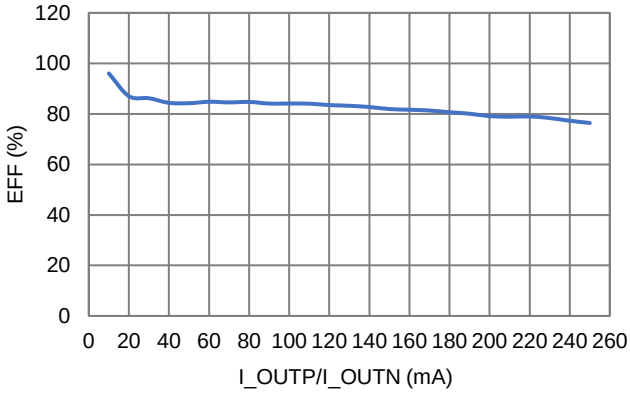
Typical Characteristics (continued)

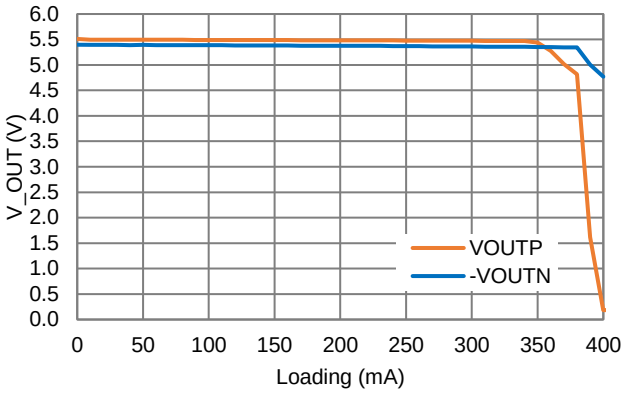
LCD Bias

V_{IN} = 3.6V, L = 2.2µH (TOKO DFE201612P-2R2M=P2), C_{IN} = C_{REG} = C_{POS} = C_{NEG} = 10µF, C_{FLY} = 4.7µF, T_A = 25°C, unless otherwise specified. Default setting V_{OUTP} = 5.5V, V_{OUTN} = -5.4V, V_{REG} = 5.8V.

Efficiency vs. Output Current

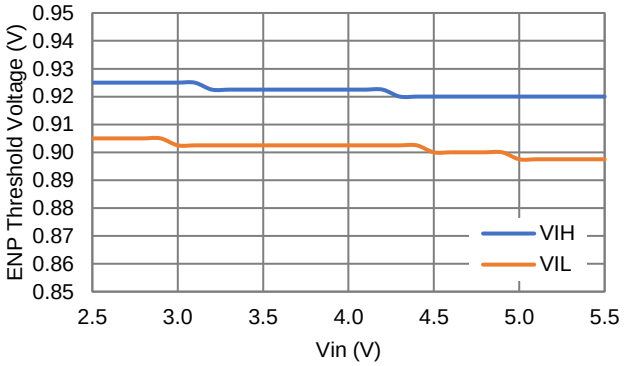


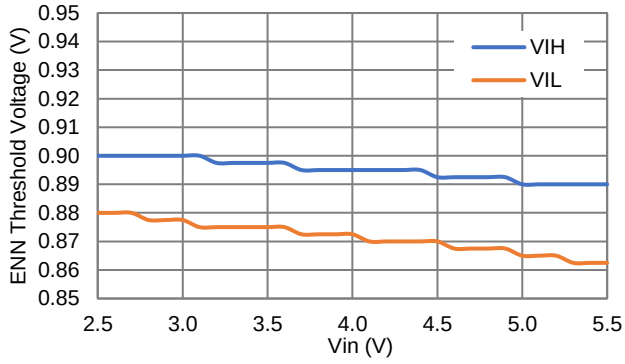
Bias V_OUT vs. Loading



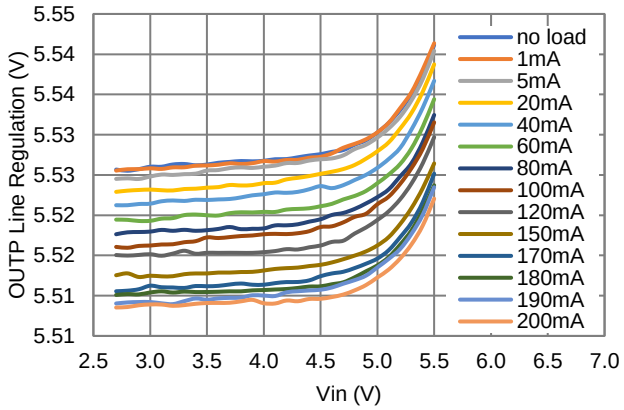
ENP/ENN Threshold vs.VIN

(Vin = 2.5V to 5.5V, VDDIO = 1.8V)

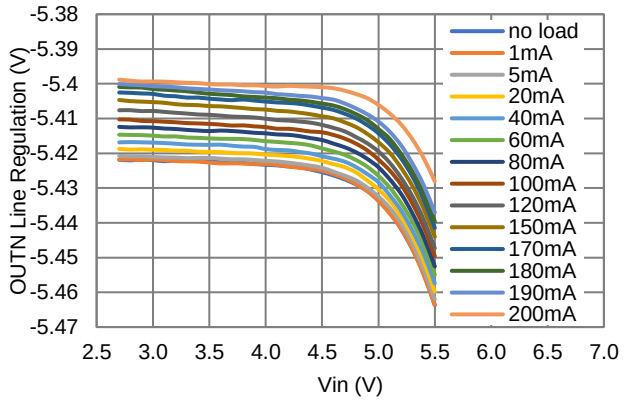




OUTP Line Regulation



OUTN Line Regulation



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Typical Characteristics (continued)

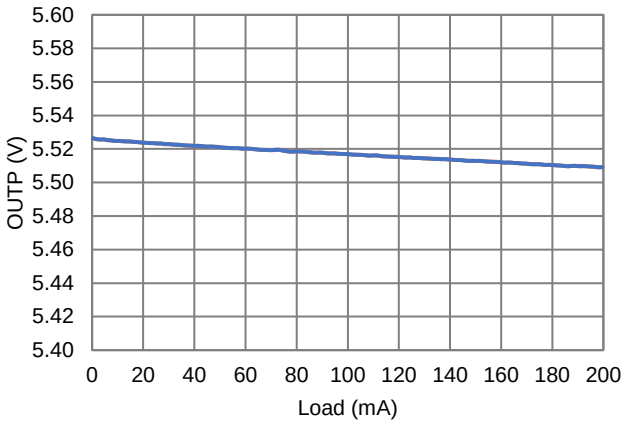
LCD Bias

V_{IN} = 3.6V, L = 2.2µH (TOKO DFE201612P-2R2M=P2), C_{IN} = C_{REG} = C_{POS} = C_{NEG} = 10µF, C_{FLY} = 4.7µF, T_A = 25°C, unless otherwise specified. Default setting V_{OUTP} = 5.5V, V_{OUTN} = -5.4V, V_{REG} = 5.8V.

Load Regulation

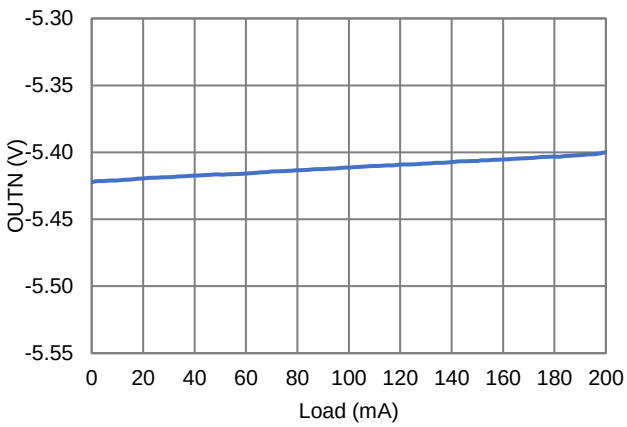
OUTP

(Vin = 3.6V, Load = 1.5mA~200mA)

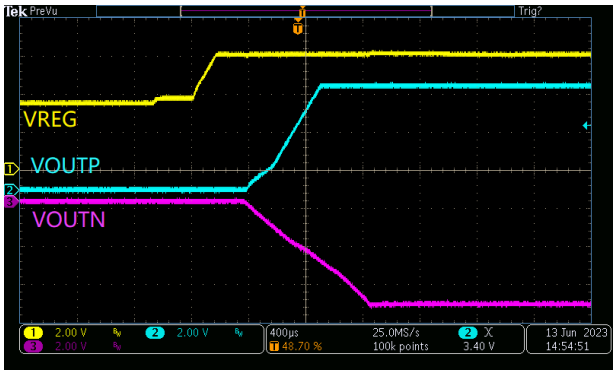


OUTN

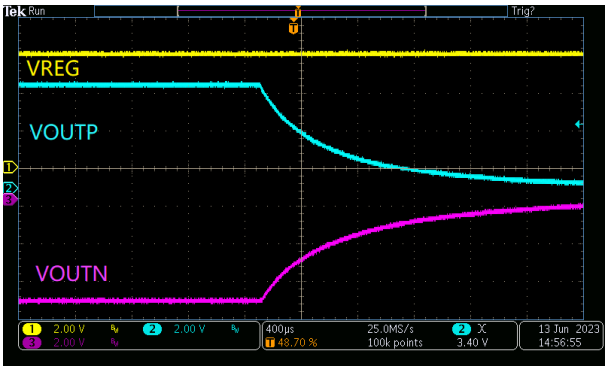
(Vin = 3.6V, Load = 1.5mA~200mA)



Power on (No Load)



Power off (No Load)



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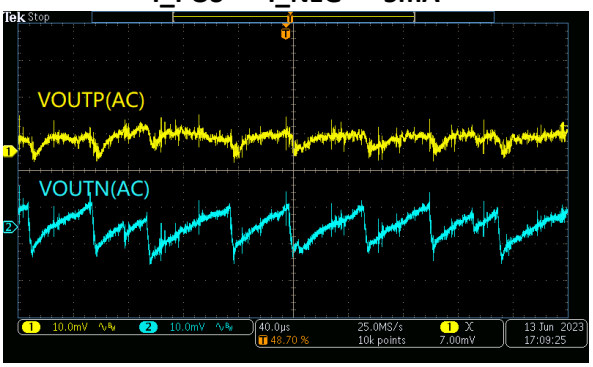
Typical Characteristics (continued)

LCD Bias

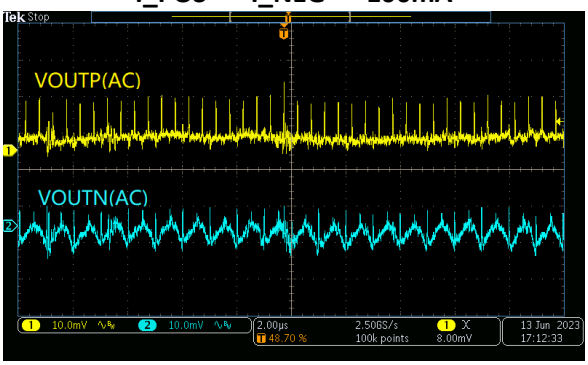
V_{IN} = 3.6V, L = 2.2µH (TOKO DFE201612P-2R2M=P2), C_{IN} = C_{REG} = C_{POS} = C_{NEG} = 10µF, C_{FLY} = 4.7µF, T_A = 25°C, unless otherwise specified. Default setting V_{OUTP} = 5.5V, V_{OUTN} = -5.4V, V_{REG} = 5.8V.

Steady State Waveforms (PWM PFM)

I_POS = -I_NEG = 5mA

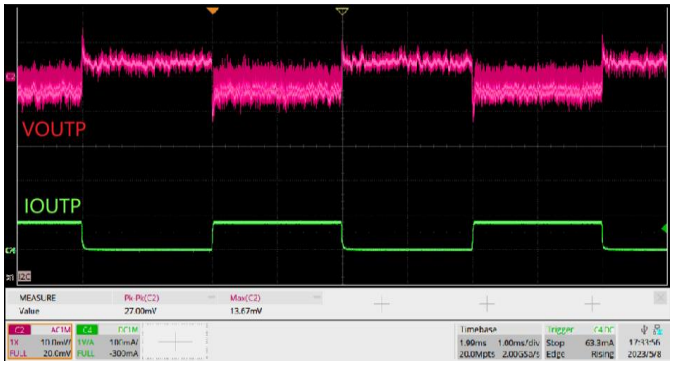


I_POS = -I_NEG = 100mA

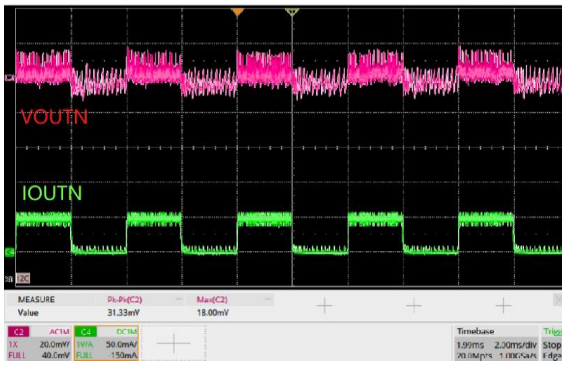


Load Transient

Step 0mA to 80mA



Step 0mA to 50mA



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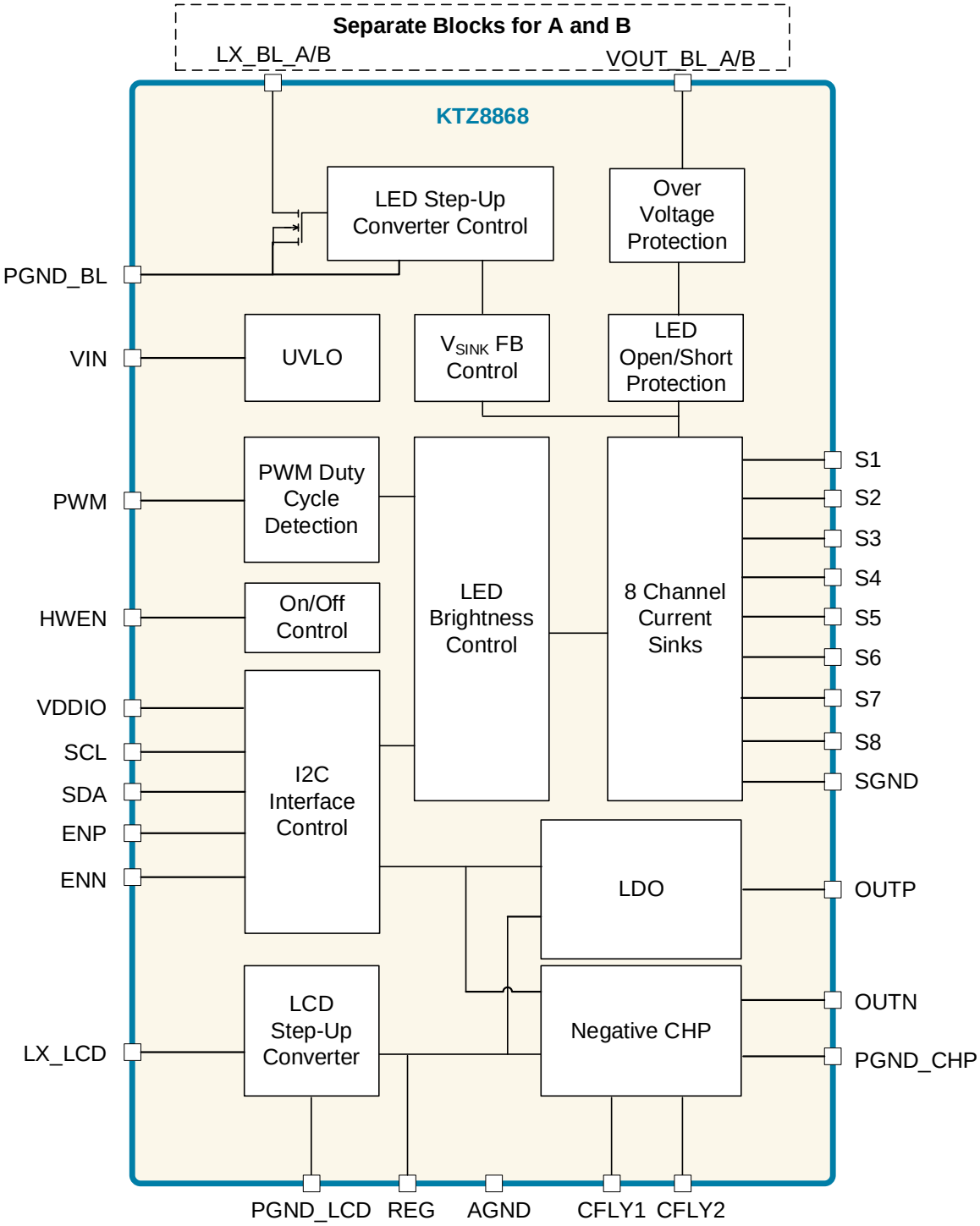
Functional Block Diagram



Functional Description

Overview

KTZ8868 is the ideal power solution for LED backlighting and LCD bias power of small and medium size panels. It integrates two step-up converters for LED backlighting, a step-up converter with LDO and inverting charge pump for LCD bias power, resulting in a simpler and smaller solution with fewer external components. High switching frequency allows the use of smaller inductors and capacitors. Its operating input ranges from 2.7V to 5.5V, accommodating 1-cell lithium-ion batteries or 5V supply.

The LED driver has two step-up converters, and each converter drivers four current sinks with total eight current sinks. Each regulated current sinks can regulate up to 30mA in backlight mode with its maximum boost output voltage up to 40V. 11bit linear or exponential I_{LED} resolution can be obtained over I^2C or PWM diming. For additional flexibility, PWM dimming offers wide range frequency and duty cycle to support Content Adaptive Brightness Control (CABC).

The LCD bias power includes a step-up converter, LDO and an inverting charge pump to generate dual outputs, OUTP and OUTN, whose voltages can be programmed via an I^2C interface. By integrating synchronous rectification MOSFETs for the step-up converter and charge pump, the KTZ8868 maximizes conversion efficiency up to 85%.

Various protection features are built into KTZ8868, including inductor current limit protection, output short circuit protection, output over-voltage protection, LED fault (open or short) protection and thermal shutdown protection. KTZ8868 is equipped with I^2C interface for various controls and status monitor.

Hardware Enable & Standby Mode

KTZ8868 has a logic input HWEN pin to enable/disable the device. When HWEN is set low, the device goes into shutdown mode, all I^2C registers are reset to default, and the I^2C interface is disabled. Under this condition, the device does not respond to any I^2C command. Even when SCL/SDA's pull up voltage is much less than VIN voltage, it will not cause any extra leakage current.

When HWEN is set high, the device goes into standby mode, the I^2C interface is enabled, and the device can respond to I^2C command.

Either HWEN input or I^2C command can be used to turn off the part, but there are some differences.

- If setting HWEN input low to turn off the part, the I_{LED} will be turned off immediately without any ramp down control. After that, the I^2C interface is disabled.
- If using an I^2C command to turn off backlight while keeping HWEN high, the I_{LED} will have ramp down control. After the LED current ramp down is finished, the I^2C interface is still alive waiting for new command.

VDDIO

KTZ8868 has VDDIO pin. By Connecting to system VDDIO with 0.1µF capacitor, the KTZ8868 can identify the IO voltage level automatically.

Backlight Boost

Two step-up converters are used to generate high voltage for driving LED strings. An adaptive control method automatically adjusts output voltage by monitoring the headroom voltage of current sinks. In this way, KTZ8868 can offer much better efficiency. The switching frequency of KTZ8868 Backlight Boost is typical 1.0MHz.

Backlight Current Sink Setting

Each current sink can be enabled or disabled by register 0x08 bits [7:0]. They can be enabled by writing the backlight enable bit to HIGH in register 0x01 bit [0] after correctly setting of LED configuration and brightness. If

a current sink is not used, connect its output to GND. During the startup, KTZ8868 will automatically detect and disable the corresponding channel.

When PWM dimming is enabled and a non-zero PWM duty cycle is detected, the KTZ8868 multiplies the duty cycle with I²C brightness settings. Figure 2 and Figure 3 describe the start-up timing for operation with I²C controlled current and with PWM controlled current.

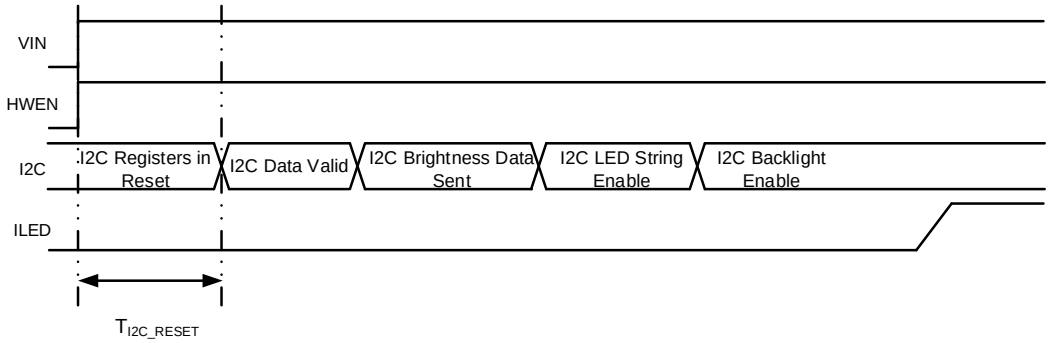


Figure 2. Enable of KTZ8868 via I²C

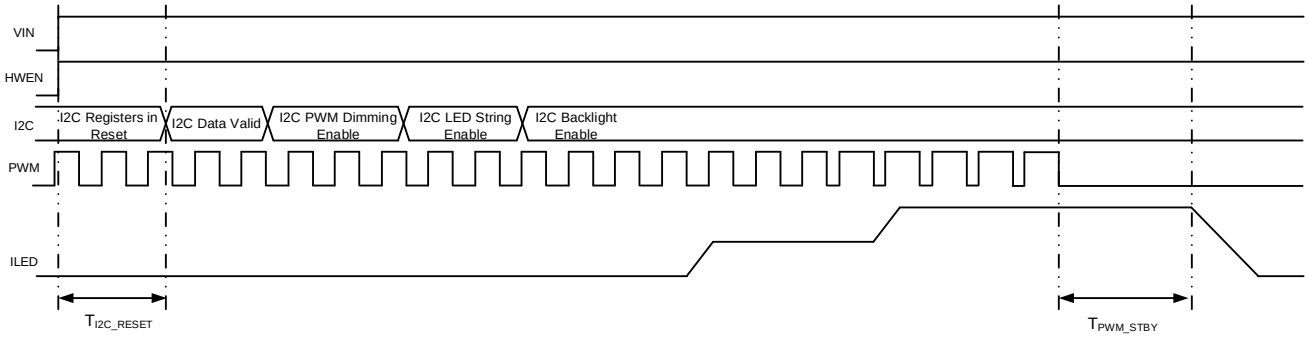


Figure 3. Enable of KTZ8868 via PWM

Operating Mode Description

The KTZ8868 backlight can operate in different modes, see Table 1 below.

Table 1. Backlight Operating Modes

HWEN	BL_EN 0x01[0]	PWM INPUT	I²C BRIGHTNESS 0X05[7:0] 0X04[2:0]	CURRENT SINKs ENABLEs 0x08[7:0]	PWM_EN 0x02[0]	FEEDBACK DISABLEs 0x10[7:0]	MAPPING MODE 0x02[3]	ACTION
0	X	X	X	X	X	X	X	Shutdown
1	0	X	X	X	X	X	X	Standby[11]
1	1	X	X	00000000	X	X	X	Standby[11]
1	1	X	0x000	X	X	X	X	Standby[11]
1	1	X	≥0x001	≥00000001	0	<11111111	0 = Exp. Mode 1 = Lin. Mode	-Backlight boost enabled -Selected current sink(s) enabled -I²C control only
1	1	Duty = 0	X	X	1	<11111111	X	Standby[11]
1	1	Duty > 0	≥0x001	≥000001	1	<11111111	0 = Exp. Mode 1 = Lin. Mode	-Backlight boost enabled -Selected current sink(s) enabled -I²C × PWM control
1	1	Duty > 0	≥0x001	≥00000001	1	11111111	0 = Exp. Mode 1 = Lin. Mode	-Backlight boost disabled -Selected current sink(s) enabled -I²C × PWM control

Backlight LED Current

The LED current is always a DC current (not PWM). It can be programmed for either exponential mapping mode or linear mapping mode by Register 0x02 bit [3]. These two modes determine the transfer characteristic of dimming code to LED current. It also has 11-bit control, including the 8-bit MSBs from register 0x05 bits [7:0] and the 3-bit LSBs from register 0x04 bits [2:0]. If only 8-bit dimming is needed, the 3-bit LSBs should be kept as '111' while the 8-bit MSBs are programmed. If 11-bit dimming ratio is needed, the 3-bit LSBs should be programmed first, then the 8-bit MSBs are programmed. Only programming the 3-bit LSBs doesn't change the current ratio until the 8-bit MSBs are programmed.

In linear mapping 8-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} * D_{PWM} * \left(\frac{3}{2050} + \frac{Code * 8 + 7}{2050}\right), \qquad (Code = 0\sim255)$$

where I_{LED_FS} is the backlight full-scale LED current which is programmed by 0x15 bits [7:3], ranges from 5.2mA to 30mA with 0.8mA step, D_{PWM} is the input PWM duty cycle if PWM dimming is enabled, otherwise $D_{PWM} = 1$.

In linear mapping 11-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} * D_{PWM} * \left(\frac{3}{2050} + \frac{Code}{2050}\right), \qquad (Code = 1\sim2047)$$

For linear mapping 11-bit dimming's Code 0, current sink and boost converter will be disabled, LED will be turned off.

11. Standby signifies that the backlight boost and current sinks are shut down. Register writes are still possible. Shutdown signifies that that the device was reset and no I2C communication is accepted.

In exponential mapping 8-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} * D_{PWM} * \frac{1.003040572^{(Code*8+7)}}{500} \quad (Code = 0\sim255)$$

In exponential mapping 11-bit dimming mode, the LED current per channel can be calculated as:

$$I_{LED\_BL} = I_{LED\_FS} * D_{PWM} * \frac{1.003040572^{Code}}{500} \quad (Code = 1\sim2047)$$

For exponential mapping 11-bit dimming's Code 0, current sink and boost converter will be disabled, LED will be turned off.

Backlight Brightness Control Mode

KTZ8868 has two brightness control mode, I²C Only Mode and I²C x PWM Mode, see Figure 4. In I²C Only Mode, register 0x02's bit [0] PWM_ENABLE should be set to "0", the LED brightness is controlled by registers 0x04 and 0x05. In I²C x PWM Mode, register 0x02's bit [0] PWM_ENABLE should be set to "1", the LED brightness will be controlled by I²C code and PWM duty together.

If the LED current is changed from one value to the other by I²C dimming Register 0x04 and Register 0x05, the ramp time can help LED current transit smoothly from one brightness level to next one. Ramp time can be adjusted from 1µs to 640ms via 0x03's bits [6:3]. Ramp time applies both to ramp up and ramp down, it remains same regardless the amount of change in brightness.

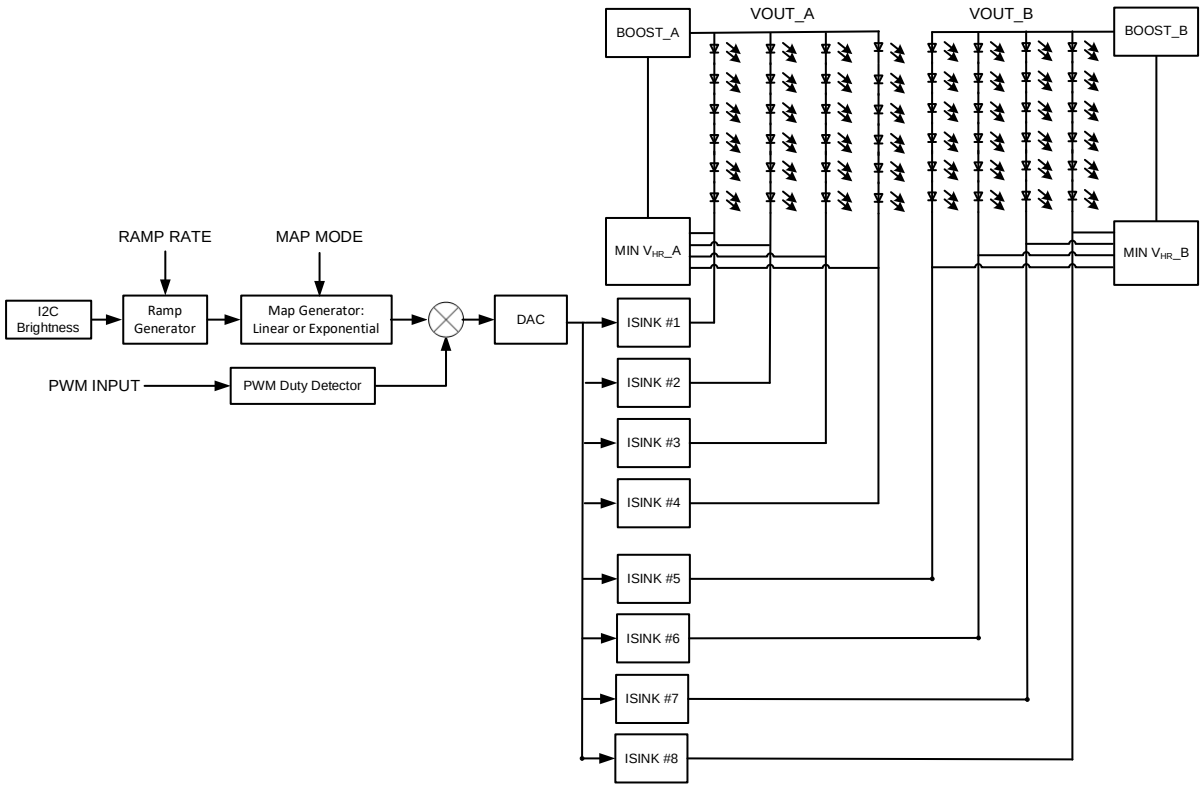


Figure 4. I²C and PWM Dimming Scheme

Backlight PWM Dimming

In backlight I²C x PWM Mode, the input PWM duty cycle is converted internally to produce a DC output sink current (not pulsing). When PWM is enabled, it can be programmed as either active high or active low by register 0x02's bit [2], with active high as default. When PWM dimming is enabled, KTZ8868 uses internal 20MHz sampling clock to detect the PWM duty cycle. It is recommended to have the minimum PWM on time as 0.1μs. For the example of 20kHz dimming frequency, the PWM duty cycle range can be 0.2%~100%. The PWM dimming frequency range can be as wide as 100Hz to 100kHz.

PWM Dimming Step Response and Timeout

If the LED current is changed from one value to the other by PWM dimming duty cycle, the transition ramp up/down time can be programmed by Register 0x15 bits [2:0]. For this transition ramp, its slope is fixed, so the final transition ramp time is dependent on the change amount of the PWM duty cycle.

The KTZ8868 PWM timeout feature turns off the boost output when the PWM is enabled and there is no PWM pulse detected.

PWM to Digital Code Readback

In I²C x PWM control mode, registers 0x12 and 0x13 contain the PWM duty cycle to the 11-bit code conversion information. Register 0x12 contains the 8 LSBs of the brightness code and register 0x13 the 3 MSBs. They are suggested to be read out in successive way to make sure the PWM duty result is correct. Too long delay between reading them may cause incorrect returned result, since input PWM duty may change during the delay time. To translate this reading to the actual LED current setting of the KTZ8868, convert it to the corresponding duty cycle and multiply it by the brightness level setting in the brightness registers (0x04 and 0x05).

Backlight PWM Hysteresis

In backlight mode, if PWM dimming frequency is high and PWM dimming duty cycle is low, even the internal fast 20MHz sampling clock's sampling error can be sufficient to cause the output LED current jitter. KTZ8868 implements PWM hysteresis control to minimize the jitter. It can be programmed by register 0x03 bits [2:0]. The input PWM duty cycle is converted to an internal 11-bit digital value, this PWM hysteresis decides how many LSBs of this 11-bit digital value is changed before the output LED current can follow the change. When PWM duty cycle changes in the same direction, no hysteresis exists. Only when the PWM duty cycle's change starts to go in different direction, does the hysteresis starts to take effect, and only when the change is larger or equal to the number of LSBs programmed, the output LED current starts to follow the change. Table 2 shows the relationship between the minimum LSB(s) and the PWM duty cycle hysteresis. Table 3 summarizes register 0x03 bits [2:0]'s minimum setting to prevent jitter under different input PWM frequency conditions. The drawback of setting PWM hysteresis too high is that the output current becomes less accurate due to the hysteresis.

Table 2. PWM Hysteresis

PWM Register 0x03 Bits [2:0]	Minimum LSB(s)	PWM Duty Cycle Hysteresis
000	0	0/2047 = 0%
001	2	2/2047 = 0.10%
010	4	4/2047 = 0.20%
011	6	6/2047 = 0.29%
100	8	8/2047 = 0.39%
101	10	10/2047 = 0.48%
110	12	12/2047 = 0.59%
111	14	14/2047 = 0.68%

Table 3. Register 0x03 Bits [2:0]'s Minimum Setting

PWM Dimming Frequency (kHz)	Sampling Error	Register 0x03 Bits [2:0]'s Minimum Setting to Prevent Jitter
0.1	0.0005%	001
1	0.005%	001
5	0.025%	001
10	0.05%	001
20	0.1%	010
40	0.2%	011
100	0.5%	110

Turn On/Off Ramp

When backlight mode is enabled from standby mode or disabled to standby mode, the LED current waveform's turn on/off time is controlled by Turn On/Off Ramp Register 0x14 bits [7:4] and bits [3:0] respectively. The 16 options range from 512µs to 16384ms, with 8ms as default. The shape of the turn on/off ramp in backlight mode can also be programmed as exponential or linear through the Register 0x02 bit [1], with linear as default.

LED Fault Protection

Each current sink is protected against LED short or open conditions. The outcome of LED short event depends on the setting of LED_SHORT_MODE bit in register 0x11 bit [2]. If it is '1' and LED short circuit condition arises, the current sink continues to regulate until $V_{SINK} > V_{SOV}$. When any sink node voltage goes above V_{SOV} (6V) for more than 59ms (typ.), LED_SHORT flag will be set in register 0x0F and that channel's current sink will be turned off, and the other channel(s) will continue to work if they don't trigger this fault condition. If it is '0', the LED_SHORT flag will be set in register 0x0F when $V_{SINK} > V_{SOV}$ more than 59ms(typ.) is detected, but KTZ8868 will keep working as usual without turning off the shorted channel's current sink until it reaches thermal shutdown.

In case of an LED failing open, the current sink voltage of the failed string will go close to ground and dominate the boost converter control loop. As a result, the output voltage will increase until it reaches the over-voltage threshold set by register 0x02 bit [7:5]. Once an OVP event has been detected, the boost will stop switching and the BL_OVP flag will be set in register 0x0F. The outcome of OVP event depends on the setting of OVP_MODE bit in register 0x02 bit [4]. If OVP_MODE is set to 0, the LED open channel will not be disabled, as soon as V_{BL_OUT} falls below the backlight OVP threshold, the KTZ8868 begins switching again, so that V_{BL_OUT} will be kept close to OVP threshold. Once the opened channel resumes to connected later, its LED current will resume and V_{BL_OUT} will go back to normal level. If OVP_MODE is set to 1, once the over-voltage incident is triggered, the BL_OVP flag is set in register 0x0F. Any of the enabled current sink headroom voltage drops below 150mV will be disabled. Then the output voltage of the boost converter will go back to normal level. During the entire process, the rest of the LED string (healthy LED string) would continue in normal operation. Even if the open channel is reconnected later, its LED current will not resume until toggling HWEN or sending software reset command or resetting backlight mode.

In case where all LED channels are open, once the output voltage of the boost converter reaches the over-voltage threshold, all the current sinks will be disabled internally, and the boost converter will stop switching. User needs to restart the IC by toggling HWEN or sending software reset command or resetting backlight mode.

Backlight Over Current Protection

The KTZ8868 has 4 different OCP thresholds (1.2A, 1.6A, 2.0A, and 2.5A) chosen by register 0x11 bits [1:0]. It is a cycle-by-cycle current limit by detecting low side power FET current. Once the threshold is trigged, the low side power FET will be turned off immediately for the rest of the switching cycle time. If enough overcurrent threshold events occur, the BL_OCP Flag (in register 0x0F) will be set.

LCD Bias Boost Converter

REG pin is the output of a high efficiency boost which is used to generate OUTP and OUTN power rails. REG boost ranges from 4V to 6.6V with 50mV step size. OUTP is generated by an LDO whose input is REG pin. OUTP ranges from 4V to 6.3V with 50mV step size and supports up to 250mA output current. OUTN is generated by an inverting charge pump whose input is REG pin. OUTN ranges from -6.3V to -4V with 50mV step size and supports up to 250mA output current. Refer to 0x0C, 0x0D, 0x0E for the settings of REG, OUTP and OUTN.

For proper operation, REG voltage is suggested to be $REG = MAX(OUTP, |OUTN|) + V_{HR}$, where $V_{HR} \geq 200mV$ for lower currents and $V_{HR} \geq 300mV$ for higher currents.

OUTP and OUTN voltage settings can be changed while they are enabled, but user must re-write register 0x09 to get new settings taking effect. The REG voltage changes immediately upon a register write. The LCD Bias outputs can be turned on/off either by ENP and ENN pins or by 0x09 register bits [2:1]. EXT_EN bit in 0x09 is used to select on/off is controlled by external pins or internal register bits. Refer to Table 4 for detailed information.

Table 4. LCD Bias Power Operating Mode

HWEN	ENN	ENP	LCD_EN_MODE 0x09[7]	OUTP_EN 0x09[2]	OUTN_EN 0x09[1]	EXT_EN 0x09[0]	ACTION
0	X	X	X	X	X	X	Device shutdown
1	0	0	0	X	X	1	Standby[12]
1	X	X	1	0	0	0	Standby[12]
1	0	1	1	X	X	1	V_{OUTP} enabled via external input
1	1	0	1	X	X	1	V_{OUTN} enabled via external input
1	1	1	1	X	X	1	V_{OUTP} and V_{OUTN} enabled via external Input
1	X	X	1	1	0	0	V_{OUTP} enabled via I^2C
1	X	X	1	0	1	0	V_{OUTN} enabled via I^2C
1	X	X	1	1	1	0	V_{OUTP} and V_{OUTN} enabled via I^2C

Fast Discharge

KTZ8868 has internal switch resistance for discharging OUTP and OUTN when device is shutdown. The OUTP discharge function is enabled with register 0x09 bit [4] and the OUTN discharge is enabled with register 0x09 bit [3].

OUTP Short Circuit Protection

If output current of OUTP is greater than 340mA (typical), the OUTP_SHORT flag will be set in register 0x0F. A I^2C readback is required to clear the flag. The outcome of an OUTP_SHORT detection depends on the setting of register 0x0A bits [7:6], including report-only flag, shutdown OUTP/OUTN, and shutdown OUTP/OUTN and backlight. KTZ8868 provides four level short circuit detection filter: 100µs, 500µs, 1ms, and 2ms by register 0x0B bits [3:2] to avoid false trigger problems.

OUTN Short Circuit Protection

OUTN_SHORT flag will be set in register 0x0F if OUTN is found shorted to ground. An I^2C readback of register 0x0F is required to clear the flag. The outcome of an OUTN_SHORT detection depends on the setting of register 0x0A bits [7:6], including report-only flag, shutdown OUTP/OUTN, and shutdown OUTP/OUTN and backlight. KTZ8868 provides four level short circuit detection filter options: 100µs, 500µs, 1ms, and 2ms by register 0x0B bits [1:0] to avoid false trigger problems.

12. Standby signifies that OUTP and OUTN are either high impedance or being internally pulled low via the active pulldown, and that the LCD boost is off. Shutdown signifies that that the device was reset and no I2C communication is accepted.

Soft Reset

All the I²C registers can be reset to their default settings by writing '1' to the SOFTWARE_RESET bit in Register 0x01, this bit will be reset to '0' automatically after the software reset.

UVLO

Under voltage lock-out (UVLO) featured is included to monitor the input voltage VIN. Once VIN drops below UVLO falling threshold, the current sinks are disabled, and the boost converters stop switching. After VIN increases above UVLO rising threshold, the boost converters and the current sinks will resume to their previous setting.

Thermal Shutdown

The KTZ8868 has Thermal Shutdown Protection which will turn off the backlight boost, all current sinks, LCD bias boost, inverting charge pump, and the LDO when the die temperature reaches or exceeds 150°C (typ). The I²C access is still available during Thermal Shutdown event, but TSD flag will be set in register 0x0F, this bit is real time reflection of TSD. When TSD is gone, the bit will be reset back to 0 automatically.

Device Functional Modes

Shutdown: The KTZ8868 is in shutdown when the HWEN pin is low. I²C writes are not recognized in shutdown.

Standby: After the HWEN pin is set high the KTZ8868 goes into standby mode. In standby mode, I²C writes are allowed but references, bias currents, the oscillator, LCD Bias, and backlight are all disabled to keep the quiescent supply current low.

Normal mode: Each of the main blocks of the KTZ8868 are independently controlled. For details on how to control each mode, see Tables 1 and 4.

Application Information

I²C Serial Data Bus

KTZ8868 supports the I²C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. KTZ8868 operates as a slave on the I²C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. KTZ8868 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL.

The following bus protocol has been defined in Figure 5:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Setup and hold times must also be taken into account.

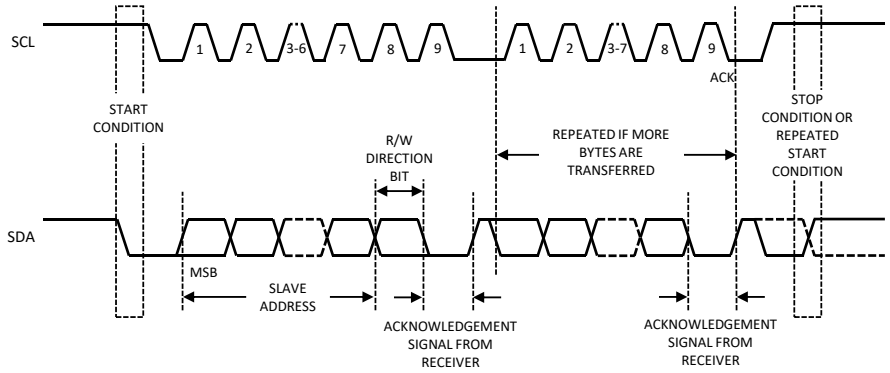


Figure 5. Data Transfer on I²C Serial Bus

KTZ8868 7-bit slave device address is 0010001 binary (0x11h).

There are two kinds of I²C data transfer cycles: write cycle and read cycle.

I²C Write Cycle

For I²C write cycle, data is transferred from a master to a slave. The first byte transmitted is the 7-bit slave address plus one bit of '0' for write. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first. Figure 6 shows the sequence of the I²C write cycle.

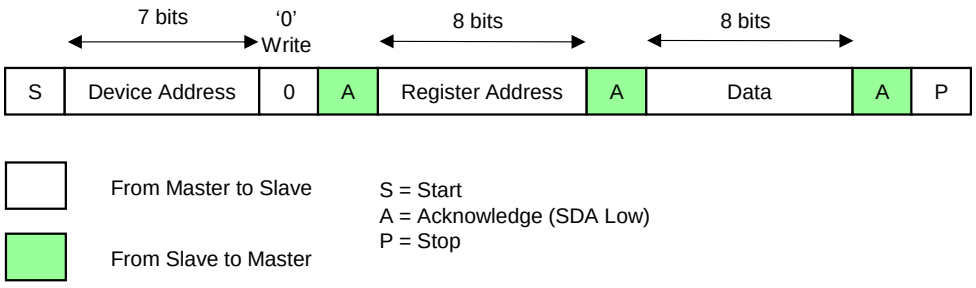


Figure 6. I²C Write Cycle

I²C Write Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0010001 for KTZ8868) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master sends 8-bit data for that addressed register.
- Slave sends acknowledge.
- If master sends more data bytes, the register address will be incremented by one after each acknowledge.
- Master generates stop condition to finish the write cycle.

I²C Read Cycle

For I²C read cycle, data is transferred from a slave to a master. But to start the read cycle, master needs to write the register address first to define which register data to read. Figure 7 shows the steps of the I²C read cycle.

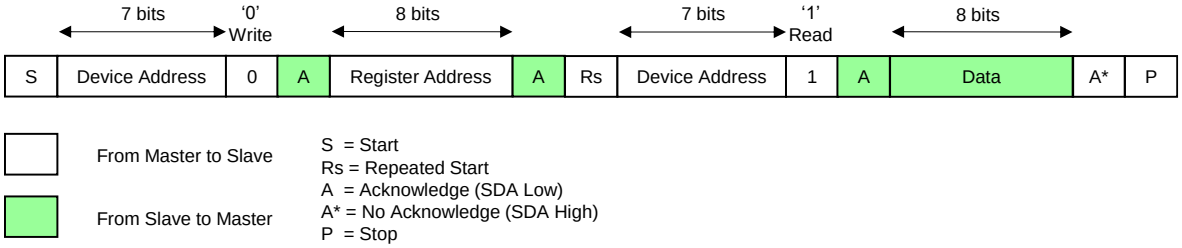


Figure 7. I²C Read Cycle

I²C Read Cycle Steps:

- Master generates start condition.
- Master sends 7-bit slave address (0010001 for KTZ8868) and 1-bit data direction '0' for write.
- Slave sends acknowledge if the slave address is matched.
- Master sends 8-bit register address.
- Slave sends acknowledge.
- Master generates repeated start condition.
- Master sends 7-bit slave address (0010001 for KTZ8868) and 1-bit data direction '1' for read.
- Slave sends acknowledge if the slave address is matched.
- Slave sends the data byte of that addressed register.
- If master sends acknowledge, the register address will be incremented by one after each acknowledge and the slave will continue to send the data for the updated addressed register.
- If master sends no acknowledge, the slave will stop sending the data.
- Master generates stop condition to finish the read cycle.

I²C Register Map

Table 5 summarizes KTZ8868's 20 I²C registers, their read/write settings and default values. They can be reset to default values by VIN power on reset, toggling HWEN or I²C software reset.

Table 5. I²C Register Map

Register Name	Address (Hex)	R/W	Default Value
Device ID	0x00	R	0x29
BACKLIGHT ENABLE	0x01	R/W	0x00
BL_CFG1	0x02	R/W	0xFA
BL_CFG2	0x03	R/W	0x8D
BL_BRT_LSB	0x04	R/W	0x07
BL_BRT_MSB	0x05	R/W	0xFF
BL_EN	0x08	R/W	0xFF
LCD_BIAS_CFG1	0x09	R/W	0x18
LCD_BIAS_CFG2	0x0A	R/W	0x11
LCD_BIAS_CFG3	0x0B	R/W	0x00
LCD_BOOST_CFG	0x0C	R/W	0x28
OUTP_CFG	0x0D	R/W	0x1E
OUTN_CFG	0x0E	R/W	0x1C
FLAG	0x0F	R	0x00
BL_OPTION1	0x10	R/W	0x00
BL_OPTION2	0x11	R/W	0x77
PWM2DIG_LSBs	0x12	R	0x00
PWM2DIG_MSBs	0x13	R	0x00
TURN_ON/OFF_RAMP	0x14	R/W	0x44
PWM_UP/DOWN_RAMP and IFS	0x15	R/W	0xF8

Table 6. Device ID Register

ADDRESS	MODE		RESET VALUE: 0x29
0x00	R		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	00	Reserved
5:3	Device ID	101	Device ID
2:0	Revision	001	Revision

Table 7. BACKLIGHT ENABLE REGISTER

ADDRESS	MODE		RESET VALUE: 0x00
0x01	R/W		
BIT	NAME	POR	DESCRIPTION
7	Software RESET	0	**0: Disable (Default)** 1: Reset (automatically returns to 0)
6	RSVD	0	Reserved, default as: 0
5	RSVD	0	Reserved, default as: 0
4	RSVD	0	Reserved, default as: 0
3	RSVD	0	Reserved, default as: 0
2	RSVD	0	Reserved, default as: 0
1	RSVD	0	Reserved, default as: 0
0	Backlight Enable	0	**0: Disable (Default)** 1: Enable (Can be reset by VPOS / VNEG short)

Note: Writing software reset bit to '1' will reset all I²C registers to their default values, then this bit will be internally reset back to '0'.

Table 8. BL_CFG1 Register

ADDRESS	MODE		RESET VALUE: 0xFA
0x02	R/W		
BIT	NAME	POR	DESCRIPTION
7:5	BL_OVP	111	Backlight OVP 000: 21.4V 001: 26.4V 010: 31.5V 011: 36.5V 100: 23.9V 101: 29.0V 110: 34.0V **111: 40.0V (Default)**
4	OVP_MODE	1	0: OVP is report only **1: OVP will turn off the fault string that causes OVP event. (Default)**
3	BLED_MAP	1	0: Exponential **1: Linear (Default)**
2	PWM_CONFIG	0	**0: Active high (Default)** 1: Active low
1	RAMP_SHAPE	1	0: Exponential **1: Linear (Default)**
0	PWM_ENABLE	0	**0: PWM disabled (Default)** 1: PWM enabled

Note: When Backlight Current Mapping setting is changed, the LED current change will not take effect until Register 0x05 is programmed.

Table 9. BL_CFG2 Register

ADDRESS	MODE		RESET VALUE: 0x8D
0x03	R/W		
BIT	NAME	POR	DESCRIPTION
7	RSVD	1	Reserved (Must be 1)
6:3	LED CURRENT RAMP	0001	Controls backlight LED ramping time. The transient time is a constant time that the backlight takes to transition from an existing programmed code to a new programmed code. 0000: 1μs **0001: 2ms (Default)** 0010: 4ms 0011: 8ms 0100: 16ms 0101: 32ms 0110: 64ms 0111: 128ms 1000: 192ms 1001: 256ms 1010: 320ms 1011: 384ms 1100: 448ms 1101: 512ms 1110: 576ms 1111: 640ms
2:0	PWM_HYST	101	Sets the minimum change in PWM input duty cycle that results in a change of backlight LED brightness level. 000: 0 LSB 001: 2 LSBs 010: 4 LSBs 011: 6 LSBs 100: 8 LSBs **101: 10 LSBs (Default)** 110: 12 LSBs 111: 14 LSBs

1. For LED CURRENT RAMP Time in the table, all the ramp times are fixed when current ramps from one level to the other except "0000" setting. For "0000" setting, the ramp slope is 1μs/step, the final ramp time is proportional to the 11-bit current steps.

Table 10. BL_BRT_LSB Register

ADDRESS	MODE		RESET VALUE: 0x07
0x04	R/W		
BIT	NAME	POR	DESCRIPTION
7:3	RSVD	00000	
2:0	BRT [2:0]	111	3-bit brightness code LSBs

Table 11. BL_BRT_MSB Register

ADDRESS	MODE		RESET VALUE: 0xFF
0x05	R/W		
BIT	NAME	POR	DESCRIPTION
7:0	BRT [7:0]	11111111	8-bit brightness code MSBs

Note:
1. If only using 8-bit current ratio, keep the 3-bit LSBs as '111' and only program the 8-bit MSBs.
2. If using 11-bit current ratio, the 3-bit LSBs should be programmed first, then the 8-bit MSBs can be programmed to take effect. Even if only the 3-bit LSBs need to be changed, the 8-bit MSB should always be programmed to make the 3-bit LSBs change taking effect.
3. For 11-bit program code 11'b00000000000, both boost converter and current sinks are turned off.

Table 12. BL_EN Register

ADDRESS	MODE		RESET VALUE: 0xFF
0x08	R/W		
BIT	NAME	POR	DESCRIPTION
7	LED8_EN	1	0 = Current sink 8 disabled **1 = Current sink 8 enabled (Default)**
6	LED7_EN	1	0 = Current sink 7 disabled **1 = Current sink 7 enabled (Default)**
5	LED6_EN	1	0 = Current sink 6 disabled **1 = Current sink 6 enabled (Default)**
4	LED5_EN	1	0 = Current sink 5 disabled **1 = Current sink 5 enabled (Default)**
3	LED4_EN	1	0 = Current sink 4 disabled **1 = Current sink 4 enabled (Default)**
2	LED3_EN	1	0 = Current sink 3 disabled **1 = Current sink 3 enabled (Default)**
1	LED2_EN	1	0 = Current sink 2 disabled **1 = Current sink 2 enabled (Default)**
0	LED1_EN	1	0 = Current sink 1 disabled **1 = Current sink 1 enabled (Default)**

Table 13. LCD_CFG1 Register

ADDRESS	MODE		RESET VALUE: 0x18
0x09	R/W		
BIT	NAME	POR	DESCRIPTION
7	LCD_EN	0	**0 = Bias supply off (I^2C and external) (Default)** 1 = Normal mode
6:5	RSVD	00	
4	OUTP_DISCH	1	0 = No pulldown on OUTP **1 = Pulldown on OUTP when in shutdown (Default)**
3	OUTN_DISCH	1	0 = No pulldown on OUTN **1 = Pulldown on OUTN when in shutdown (Default)**
2	OUTP_EN	0	**0 = OUTP disabled (Default)** 1 = OUTP enabled
1	OUTN_EN	0	**0 = OUTN disabled (Default)** 1 = OUTN enabled
0	EXT_EN	0	Activates external enables (ENP and ENN) **0 = External enables are disabled. OUTP and OUTN can only be enabled via bit OUTP_EN and OUTN_EN, respectively (Default)** 1 = External enables are enabled. OUTP and OUTN can only be enabled via pin ENP and ENN, respectively.

Table 14. LCD_CFG2 Register

ADDRESS	MODE		RESET VALUE: 0x11
0x0A	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	BIAS_SHORT_MODE	00	**0X = Flag only (Default)** 10 = Flag + shutdown V_{OUTP}/V_{OUTN} 11 = Flag + shutdown V_{OUTP}/V_{OUTN}/Backlight
5:4	VOUTP_RAMP	01	V_{OUTP} ramp time, low to high: 00 = 228µs **01 = 456µs (Default)** 10 = 684µs 11 = 912µs
3:0	VOUTN_RAMP	0001	V_{OUTN} ramp time, high to low: 0000 = 456µs **0001 = 912µs (Default)** 0010 = 1368µs 0011 = 1824µs 0100 = 2280µs 0101 = 2736µs 0110 = 3192µs 0111 = 3648µs 1000 = 4104µs 1001 = 4560µs 1010 = 5016µs 1011 = 5472µs 1100 = 5928µs 1101 = 6384µs 1110 = 6840µs 1111 = 7296µs

Note:

1. For VOUTP_RAMP time, it is fixed slew rate ramp strategy, the ramp time value is given by assuming OUTP = 5.75V. If OUTP is set 5.5V and VOUTP_RAMP = 01, then actual ramp time will be 456*5.5/5.75 = 436µs.
2. For VOUTN_RAMP time, it is fixed slew rate ramp strategy, the ramp time value is given by assuming OUTN = -5.75V. If OUTN is set -5.5V and VOUTN_RAMP = 0001, then actual ramp time will be 912*5.5/5.75 = 872µs.

Table 15. LCD_CFG3 Register

ADDRESS	MODE		RESET VALUE: 0x00
0x0B	R/W		
BIT	NAME	POR	DESCRIPTION
7:4	RSVD	0000	
3:2	VOUTP_SC_FILT	00	OUTP short circuit filter timer **00 = 2ms (Default)** 01 = 1ms 10 = 500µs 11 = 100µs
1:0	VOUTN_SC_FILT	00	OUTN short circuit filter timer **00 = 2ms (Default)** 01 = 1ms 10 = 500µs 11 = 100µs

Table 16. LCD_BOOST_CFG Register

ADDRESS	MODE		RESET VALUE: 0x28
0x0C	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	00	
5:0	REG	101000	REG voltage (50-mV steps): REG = 4V + (Code × 50mV) 000000 : 4V 000001 : 4.05V : **101000 : 6V (Default)** : >=110100 : 6.6V

Table 17. OUTP_CFG Register

ADDRESS	MODE		RESET VALUE: 0x1E
0x0D	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	00	
5:0	OUTP	011110	OUTP voltage (50mV steps): V_{OUTP} = 4V + (Code × 50mV), 6.3V max 000000 : 4V 000001 : 4.05V : **011110 : 5.5V (Default)** : >=101110 : 6.3V

Note: Writing to Register 0x0D will not take effect immediately, until Register 0x09 is written again.

Table 18. OUTN_CFG Register

ADDRESS	MODE		RESET VALUE: 0x1C
0x0E	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	RSVD	00	
5:0	OUTN	011100	OUTN voltage (–50mV steps): V_{OUTN} = -4 V - (Code × 50mV), -6.3V min 000000 : –4 V 000001 : –4.05V : **011100 : –5.4V (Default)** : >=101110 : –6.3V

Note: Writing to Register 0x0E will not take effect immediately, until Register 0x09 is written again.

Table 19. FLAG Register

ADDRESS	MODE		RESET VALUE: 0x00
0x0F	R		
BIT	NAME	POR	DESCRIPTION
7	LED_SHORT	0	**0 = Normal operation** 1 = LED short protection trigged
6	TSD	0	**0 = Normal operation** 1 = Thermal shutdown triggered (die temperature > 150°C)
5	OUTP_SHORT	0	**0 = Normal operation** 1 = OUTP output has hit the overcurrent threshold
4	OUTN_SHORT	0	**0 = Normal operation** 1 = OUTN > 0.9 × V_{OUTN_target}
3	BL_GROUPB_OVP	0	**0 = Normal operation** 1 = Backlight boost outputB > OVP threshold
2	BL_GROUPA_OVP	0	**0 = Normal operation** 1 = Backlight boost outputA > OVP threshold
1	BL_GROUPB_OCP	0	**0 = Normal operation** 1 = Backlight boost outputB switch current > OCP threshold
0	BL_GROUPA_OCP	0	**0 = Normal operation** 1 = Backlight boost outputA switch current > OCP threshold

Note:
1. TSD is real-time results.
2. LED_SHORT, OUTP_SHORT, OUTN_SHORT, BL_OVP and BL_OCP are latched results; OUTP_SHORT, OUTN_SHORT, BL_OVP and BL_OCP can be reset by reading back 0x0F.
3. All the status bits can be reset by VIN power on reset, software reset or toggling HWEN.

Table 20. BL_OPTION1 Register

ADDRESS	MODE		RESET VALUE: 0x00
0x10	R/W		
BIT	NAME	POR	DESCRIPTION
7	LED8_FB_DISABLE	0	**0 = Feedback enabled (Default)** 1 = Feedback disabled
6	LED7_FB_DISABLE	0	**0 = Feedback enabled (Default)** 1 = Feedback disabled
5	LED6_FB_DISABLE	0	**0 = Feedback enabled (Default)** 1 = Feedback disabled
4	LED5_FB_DISABLE	0	**0 = Feedback enabled (Default)** 1 = Feedback disabled
3	LED4_FB_DISABLE	0	**0 = Feedback enabled (Default)** 1 = Feedback disabled
2	LED3_FB_DISABLE	0	**0 = Feedback enabled (Default)** 1 = Feedback disabled
1	LED2_FB_DISABLE	0	**0 = Feedback enabled (Default)** 1 = Feedback disabled
0	LED1_FB_DISABLE	0	**0 = Feedback enabled (Default)** 1 = Feedback disabled

Note: If all LED1~LED4 feedback disabled, Boost_A stops switching. If all LED5~LED8 feedback disabled, Boost_B stops switching.

Table 21. BL_OPTION2 Register

ADDRESS	MODE		RESET VALUE: 0x77
0x11	R/W		
BIT	NAME	POR	DESCRIPTION
7:6	BL_L_SELECT	01	00 = 6.8μH **01 = 4.7μH (Default)** 10 = 10μH 11 = 10μH
5:4	RSVD	11	
3	RSVD	0	
2	LED_SHORT_MODE	1	0 = Keep fault string on **1 = Turn off fault string (Default)**
1:0	BL_CURRENT_LIMIT	11	00 = 1.2A 01 = 1.6A 10 = 2.0A **11 = 2.5A (Default)**

Table 22. PWM2DIG_LSBs Register

ADDRESS	MODE		RESET VALUE: 0x00
0x12	R		
BIT	NAME	POR	DESCRIPTION
7:0	PWM_TO_DIG	00000000	11-bit PWM-to-digital conversion code LSBs

Table 23. PWM2DIG_MSBs Register

ADDRESS	MODE		RESET VALUE: 0x00
0x13	R		
BIT	NAME	POR	DESCRIPTION
7:3	RSVD	00000	
2:0	PWM_TO_DIG	000	11-bit PWM-to-digital conversion code MSBs

Note: 0x12 and 0x13 are suggested to be read out in successive way to make sure the PWM duty result is correct. Too long delay between reading them may cause incorrect returned result, since input PWM may change during the delay time.

Table 24. TURN_ON/OFF_RAMP Register

ADDRESS	MODE		RESET VALUE: 0x44
0x14	R/W		
BIT	NAME	POR	DESCRIPTION
7:4	RAMP_ON_TIME	0100	On Ramp Time 0000 : 512µs 0001 : 1ms 0010 : 2ms 0011 : 4ms **0100 : 8ms (Default)** 0101 : 16ms 0110 : 32ms 0111 : 64ms 1000 : 128ms 1001 : 256ms 1010 : 512ms 1011 : 1024ms 1100 : 2048ms 1101 : 4096ms 1110 : 8192ms 1111 : 16384ms
3:0	RAMP_OFF_TIME	0100	Off Ramp Time 0000 : 512µs 0001 : 1ms 0010 : 2ms 0011 : 4ms **0100 : 8ms (Default)** 0101 : 16ms 0110 : 32ms 0111 : 64ms 1000 : 128ms 1001 : 256ms 1010 : 512ms 1011 : 1024ms 1100 : 2048ms 1101 : 4096ms 1110 : 8192ms 1111 : 16384ms

Table 25. PWM_UP/DOWN_RAMP Register

ADDRESS	MODE		RESET VALUE: 0xF8
0x15	R/W		
BIT	NAME	POR	DESCRIPTION
7:3	IFS	11111	Backlight Full-scale LED Current ILED_FS ILED_FS = 5.2+Code*0.8mA **11111 : 30mA (Default)** …. 10100 : 21.2mA 10011 : 20.4mA 10010: 19.6mA .... 00010 : 6.8mA 00001 : 6.0mA 00000 : 5.2mA
2:0	PWM_RAMP_TIME	000	PWM Duty Cycle Transition Ramp Time **000 : 2ms (Default)** 001 : 4ms 010 : 8ms 011 : 16ms 100 : 32ms 101 : 64ms 110 : 128ms 111 : 256ms

Note: The PWM Dimming Transition Ramp Time in the table is defined as the time to change between minimum PWM duty cycle and the maximum PWM duty cycle. The final transition time is the multiplication of the time in the table and the change of the PWM duty cycle.

Capacitor Selection for Backlight Driver

Small size ceramic capacitors with low ESR are ideal for all applications. A 10µF input capacitor and a 1µF output capacitor are suggested. The voltage rating of these capacitors should exceed the maximum possible voltage at the corresponding pins, and these capacitors should be as close as possible to the IC. Table 25 shows the recommended capacitor vendors.

Table 26. Recommended Capacitor Vendors

Manufacturer	Website
Murata	www.murata.com
AVX	www.avx.com
Taiyo Yuden	www.t-yuden.com

Inductor Selection for Backlight Driver

An inductor of 4.7µH to 10µH with low DCR can be selected for the boost converter. To decide the current rating of the inductor required for the application, the following equation can be used to estimate the peak inductor current I_{PEAK} in continuous conduction mode (CCM):

$$I_{PEAK} = \frac{V_{OUT(MAX)} \times I_{OUT(MAX)}}{V_{IN(MIN)} \times \eta} + \frac{V_{IN(MIN)}}{2L \times F_{SW}} \times \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}\right)$$

where $V_{OUT(MAX)}$ is the maximum output voltage, $V_{IN(MIN)}$ is the minimum input voltage, $I_{OUT(MAX)}$ is the maximum output current, F_{SW} is the boost converter's switching frequency, L is the inductor value, η is the boost converter's efficiency under that condition. **Table 27** shows recommended inductors under different application conditions.

Table 27. Recommended Inductors

Value (µH)	Manufacturer	Inductor Part Number	DCR (Ω)	Saturation Current (A)	EIA Size (mm)
4.7	TDK	VLS3012HBX-4R7M	0.175	2.51	3.0×3.0×1.2
4.7	TAIYO YUDEN	NRS6028T 4R7MMGK	0.031	2.7	6.0×6.0×2.8

Schottky Diode Selection

Using a schottky diode is recommended because of its low forward voltage drop and fast reverse recovery time. The average current rating of the schottky diode should exceed the maximum output current, and its peak current rating should exceed the peak inductor current. Its voltage rating should also exceed the OVP setting. **Table 28** shows the recommended schottky diode.

Table 28. Recommended Schottky Diode

Application	Schottky Diode Part Number	Forward Voltage (V)	Forward Current (A)	Reverse Voltage (V)	Manufacturer
All	PMEG6010CEGWX	0.57	1	60	Nexperia

Capacitor Selection for Dual Output Bias

Small size ceramic capacitors with low ESR are ideal for all applications. A 10µF output capacitor at REG are suggested. Higher capacitor values can be used to improve the load transient response. The voltage rating of these capacitors should exceed the maximum possible voltage at the corresponding pins, and these capacitors should be as close as possible to the IC.

Flying Capacitor Selection for Bias

The charge pump needs an external flying capacitor. The minimum value for smartphone application is 4.7µF and 10µF for tablet application. Special care must be taken while choosing the flying capacitor as it will directly impact the output voltage accuracy and load regulation performance.

Inductor Selection for Dual Output Bias

An inductor in the range of 2.2µH to 10µH with low DCR can be selected for the boost converter. To estimate the inductance required for applications, calculate the maximum input average current as the following

$$I_{IN(MAX)} = \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Where, η is the converter efficiency and can be approximated as 90% for the typical case. In order to have smaller current ripple (to improve efficiency and minimize output voltage ripple), larger inductance will be required. If inductor ripple current needs to be less than 40% of the average input current, then

$$\Delta I_L = \frac{V_{IN} \cdot D \cdot T_S}{L} \le 40\% \cdot \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Where duty cycle can be estimated as

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Then

$$\Delta I_L = \frac{V_{IN} \cdot (V_{OUT} - V_{IN}) \cdot T_S}{L \cdot V_{OUT}} \le 40\% \cdot \frac{V_{OUT} \cdot I_{OUT(MAX)}}{V_{IN} \cdot \eta}$$

Therefore, the inductance can be calculated as

$$L \ge \frac{V_{IN}^2 \cdot (V_{OUT} - V_{IN}) \cdot \eta}{40\% \cdot V_{OUT}^2 \cdot I_{OUT(MAX)} \cdot f_S}$$

Where, f_S is the switching frequency of the boost converter.

Table 28. Recommended Inductor Part Numbers

Value (µH)	Manufacturer	Inductor Part Number	DCR (Ω)	Saturation Current (A)	EIA Size (mm)
2.2	Toko	DFE201612P-2R2M	0.12	2.1	2 x 1.6 x 1.0
2.2	CYCTEC	HMLQ25201T-2R2MSR	0.102	3	2.5 x 2.0 x 1.0

Recommended PCB Layout

PCB layout is very important for high frequency switching regulators in order to keep the loop stable and minimize noise. The input capacitor (C_{IN}) should be very close to the IC's VIN pin and PGND pin in order to get the best decoupling. The path between the inductor, LX pin, schottky diode and the output capacitor (C_{OUT}) should be kept as short as possible to minimize noise and ringing. To reduce power loss, the trace through the inductor, LX pin, schottky diode and C_{OUT} should be as short and wide as possible. Both input and output capacitors' GND terminals should be connected together on the PCB top layer and on the bottom layer GND plane.

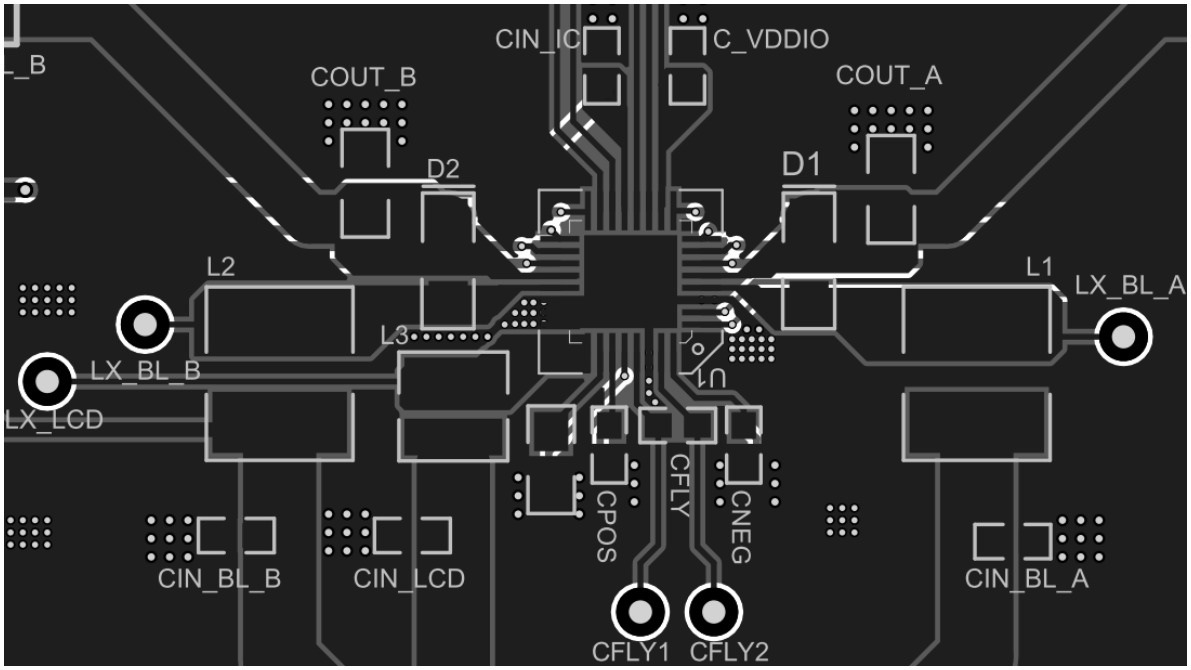
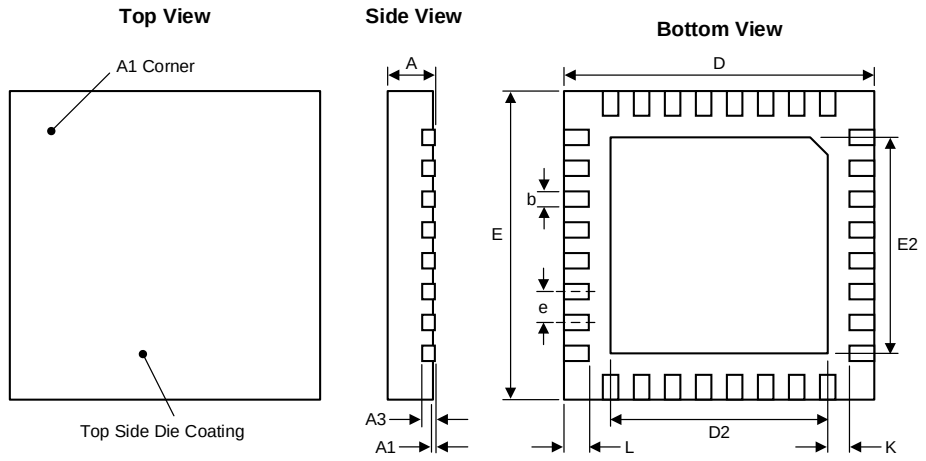


Figure 8. Recommended PCB Layout

Packaging Information

WQFN55-32 (5.00mm x 5.00mm x 0.75mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.45	3.50	3.55
E	4.90	5.00	5.10
E2	3.45	3.50	3.55
e		0.50 BSC	
K	0.20	–	–
L	0.35	0.40	0.45

Recommended Footprint