3-phase BLDC Motor Controller for 6-wire

Features

- Built-in Vector Engine controller
- Sensorless Field Oriented Control
- Sensorless Direct Torque Control
- Initial Position Detection
- Initial Speed Detection
- Smart start-up method
- 12-bit ADC converters
- I²C interfaces
- QFN48L 6mm x 6mm x 0.75mm

Applications

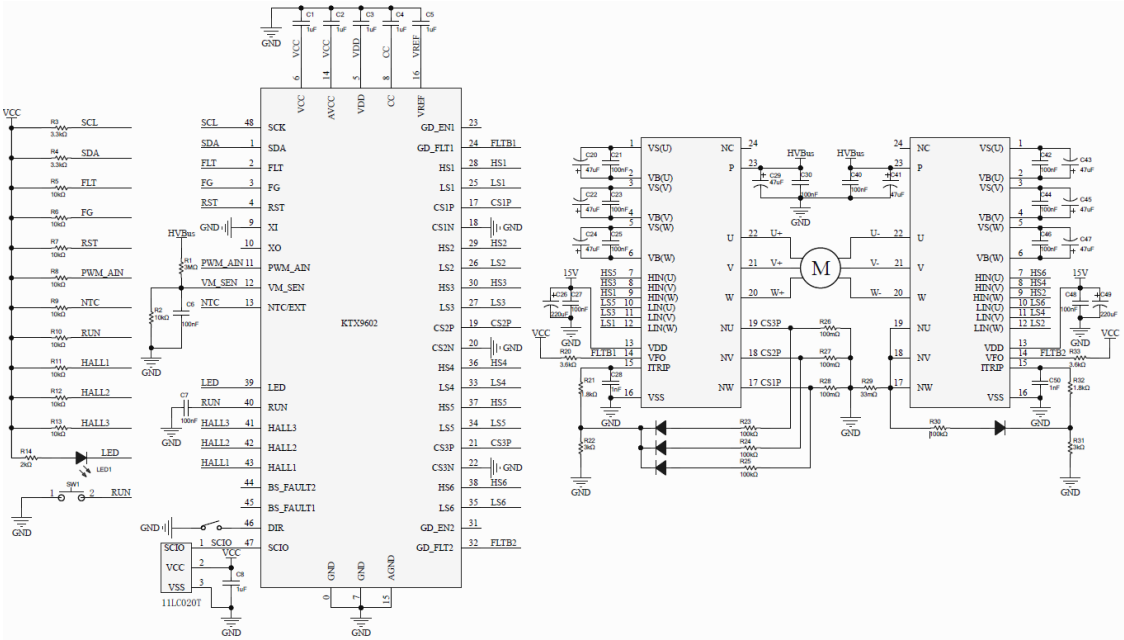
- Brushless DC Motors (sinusoidal PMSM)
- Home appliance and air-con fans
- Battery Operated devices
  - Portable vacuum cleaners
  - Power Tools, etc.
- Drones and aero modeling
- EV non-drivetrain

Brief Description

The KTX9602 is a motor controller IC, the third-generation solution in Kinetics' patented PURESINE™ 6-wire technology family. Specifically designed for all sinusoidal Permanent Magnet Synchronous Motor (PMSM) 6-wire PURESINE™ 3 Phase BLDC motors, offering the unique benefits of a monolithic hybrid ASIC architecture with advanced control, monitoring, torque, speed and position detection.

The KTX9602 motor controller has built-in vector engine optimized for PMSM/BLDC applications. Designed for ease of use, the KTX9602 offers simplicity in configuration with state-of-the-art control.

Typical Application



Pin Descriptions

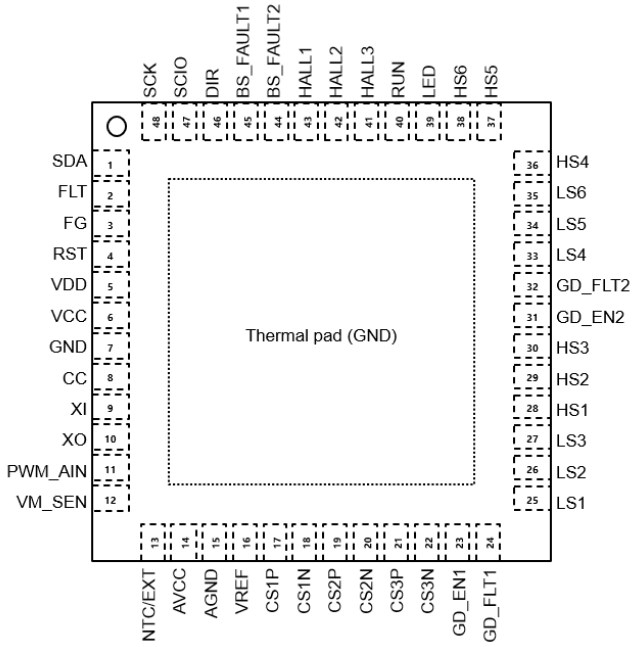
Pin #	Name	Type	Function
1	SDA	DIO	I^2C serial data input/output
2	FLT	DO	Fault alert output
3	FG	DO	FG signal pulse output
4	RST	DI	Reset
5	VDD	PWR	Internal 1.8V digital core voltage (this output must be blocked with a ceramic capacitor). This is an output and may drive external loads not to exceed to I_{LMT}
6	VCC	PWR	Device supply voltage (3.3V-5V)
7	GND	PWR	Ground
8	CC	AIO	Internal oscillator feedback. The compensation capacitor must connect to GND
9	XI	XI	External Crystal oscillator (Optional)
10	XO	XO	External Crystal oscillator (Optional)
11	PWM_AIN	AI	PWM Duty or Analog command input for selected PMODE control
12	VM_SEN	AI	DC bus voltage sensing input
13	NTC/EXT	AI	External thermistor input/External sensor analog input
14	AVCC	PWR	Analog Supply voltage (3.3V-5V)
15	AGND	PWR	Analog Ground
16	VREF	AO	Reference voltage of ADC
17	CS1P	AI	Current sense positive input channel 1
18	CS1N	AI	Current sense negative input channel 1
19	CS2P	AI	Current sense positive input channel 2
20	CS2N	AI	Current sense negative input channel 2
21	CS3P	AI	Current sense positive input channel 3
22	CS3N	AI	Current sense negative input channel 3
23	GD_EN1	DO	Enable control for Gate Driver 1
24	GD_FLT1	DI	Fault signal from Gate Driver 1
25	LS1	DO	Low side PWM output - channel 1
26	LS2	DO	Low side PWM output - channel 2
27	LS3	DO	Low side PWM output - channel 3
28	HS1	DO	High side PWM output - channel 1
29	HS2	DO	High side PWM output - channel 2
30	HS3	DO	High side PWM output - channel 3
31	GD_EN2	DO	Enable control for Gate Driver 2
32	GD_FLT2	DI	Fault input signal from Gate Driver 2
33	LS4	DO	Low side PWM output - channel 4
34	LS5	DO	Low side PWM output - channel 5
35	LS6	DO	Low side PWM output - channel 6
36	HS4	DO	High side PWM output - channel 4
37	HS5	DO	High side PWM output - channel 5
38	HS6	DO	High side PWM output - channel 6
39	LED	DO	RUN/STOP indicator signal – 0: RUN, 1: STOP
40	RUN	DI	RUN/STOP command input
41	HALL3	DI	Digital Hall sensor input 3
42	HALL2	DI	Digital Hall sensor input 2

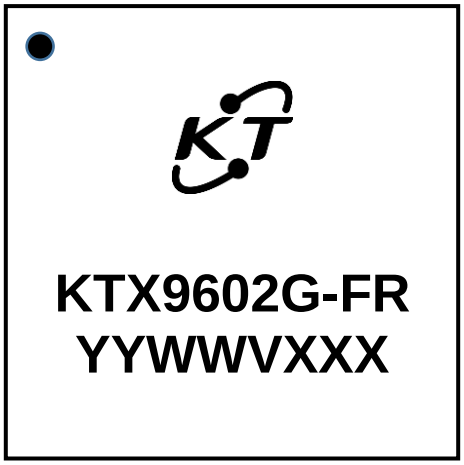
Pin #	Name	Type	Function
43	HALL1	DI	Digital Hall sensor input 1
44	BS_FAULT2	DIO	Bridge-switch fault status bus 2
45	BS_FAULT1	DIO	Bridge-switch fault status bus 1
46	DIR	DI	CW/CCW rotation direction selection
47	SCIO	DIO	External 1-Wire EEPROM interface, Serial Clock, Data input/output
48	SCK	DI	I^2C serial clock input

DI: Digital input
DO: Digital output
DIO: Digital input and output

AI: Analog input
AO: Analog output
AIO: Analog input and output
PWR: Power supply pin

WQFN66-48





48-Pin 6mm x 6mm x 0.75mm
WQFN Package
Top Mark
FR = ROM Code
YY = Year Code, WW = Week Code, V = Factory Code, XXX = Lot Sequence #

Absolute Maximum Ratings[1]

(All voltage ratings are reference to ground (GND) unless specified)

Symbol	Description	Value	Units
V_{CC}	VCC Supply Voltage	-0.3 to 6.0	V
V_{DD}	VDD Supply Voltage	-0.3 to 2.1	V
V_{CCIO}	VCC Pin Group	-0.3 to 6.0	V
V_{CSI}	Current Sense Input	-2.0 to 2.0	V
I_{SCR}	Latch-up Immunity	±100	mA
T_{STRG}	Storage Temperature	-40 to 125	°C
T_{BODY}	Package Body Temperature	260	°C

ESD Ratings

Symbol	Description	Value	Units
V_{ESDH}	ANSI/ESDA/JEDEC JS-001 Human Body Model[2]	±2	kV
	JEDEC JESD22-C101 Charge Device Model	±1	

Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	26.4	°C/W
P_D	Maximum Power Dissipation at T_A = 25°C	4.73	W
$\Delta P_D/\Delta_T$	Derating Factor above T_A = 25°C	-37.9	mW/°C

Ordering Information

Part Number[4]	Marking[5]	Ambient Operating Temperature	Package
KTX9602GUAM-AA-TE	YYWWVXXX	-40°C to +125°C	WQFN66-48

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
4. Will be qualified to a minimum MSL3.
5. YY = Year Code, WW = Week Code, V = Factory Code, XXX = Lot Sequence #.

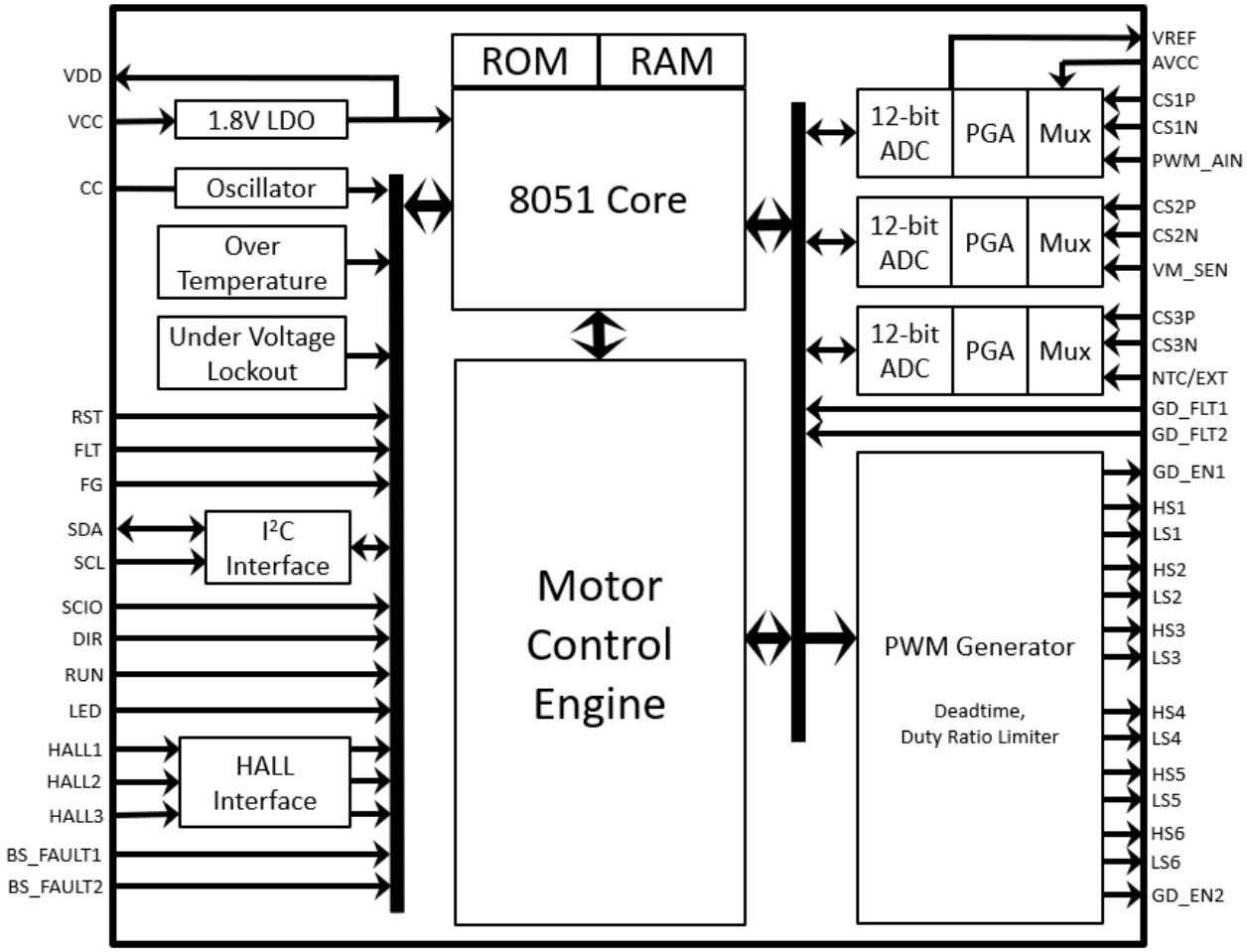
Electrical Characteristics[6]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full ambient operating temperature range of –40°C to +125°C, while *Typ* values are specified at room temperature (25°C). V_{CC} = 3.3V

Symbol	Description	Conditions	Min	Typ	Max	Units
System						
V_{SUB}	Substrate Voltage	Thermal dissipation pad	0		0	V
T_{SD}	Thermal Shutdown			150		°C
V_{CC}	Operating Voltage	VCC pin	3.0		5.5	V
I_{CC}	Operating Current	Disabled (CE = 0V)			3.0	uA
		Sleep mode		0.15		mA
		Quiescent mode		11.8		mA
		Active mode		18.6		mA
V_{CCUV}	VCC Undervoltage	VCC falling		2.4		V
V_{CCHYS}	VCC Hysteresis			0.05		V
V_{DD}	VDD Voltage		1.62	1.8	1.98	V
I_{LMT}	VDD Current Limit	V_{DD} = 1.5V		100		mA
I_{SC}		V_{DD} = 0V		40		mA
V_{DDUV}	VDD Undervoltage	V_{DD} falling		1.5		V
V_{DDHYS}	VDD Hysteresis			0.05		V
f_{OSC}	Master Clock		44.7	47.0	49.3	MHz
f_{PWM}	PWM frequency			22.9		kHz
AD Converter						
V_{FS1}	Full Scale Input	ad_range[1:0]: 2'b00		±1.0		V
V_{FS2}		ad_range[1:0]: 2'b01		±0.5		V
V_{FS4}		ad_range[1:0]: 2'b10		±0.25		V
V_{FS8}		ad_range[1:0]: 2'b11		±0.125		V
R_{FS1}	Input Resistance	ad_range[1:0]: 2'b00		10		kΩ
R_{FS2}		ad_range[1:0]: 2'b01		10		kΩ
R_{FS4}		ad_range[1:0]: 2'b10		10		kΩ
R_{FS8}		ad_range[1:0]: 2'b11		10		kΩ
	Resolution	AD only, exclude current sense amplifier circuit		12		Bits
INL	Integral Linearity	AD only, exclude current sense amplifier circuit		±4.0		LSB
DNL	Differential Linearity	AD only, exclude current sense amplifier circuit		±1.0		LSB
E_O	Offset Error	AD only, exclude current sense amplifier circuit		±4.0		LSB
f_{SPS}	Sampling Rate			250		kSPS

6. KTX9602G is guaranteed to meet performance specifications over the –40°C to +125°C ambient operating temperature range by design, characterization and correlation with statistical process controls.

Functional Block Diagram



Functional Description

Supply Voltage

VCC (3.3V~5V) is the input voltage of the system and VDD (1.8V) is generated by internal LDO regulator. VCC is used by the I/O pads, PLL and ADC. VDD is mainly used by internal digital core, also can drive external loads not to exceed I_{LMT} listed in the *Electrical Characteristics.*

Startup and System Clock

The KTX9602 will start operation when chip-enable (RST) pin is tied high and the supply voltages (VCC and VDD) are higher than the low voltage thresholds. Three different clock sources can be used to generate the system clock. After power-on, the KTX9602 will start the crystal oscillator first. If external crystal is connected to XI and XO pins, crystal oscillator can be started and will be used as clock reference. Otherwise, internal oscillator will be used instead. If external clock source is fed to XI pin during startup, the clock source will be used as clock reference. KTX9602 will also undergo startup routine every time wake up from sleep mode.

State Diagram (Startup and Sleep)

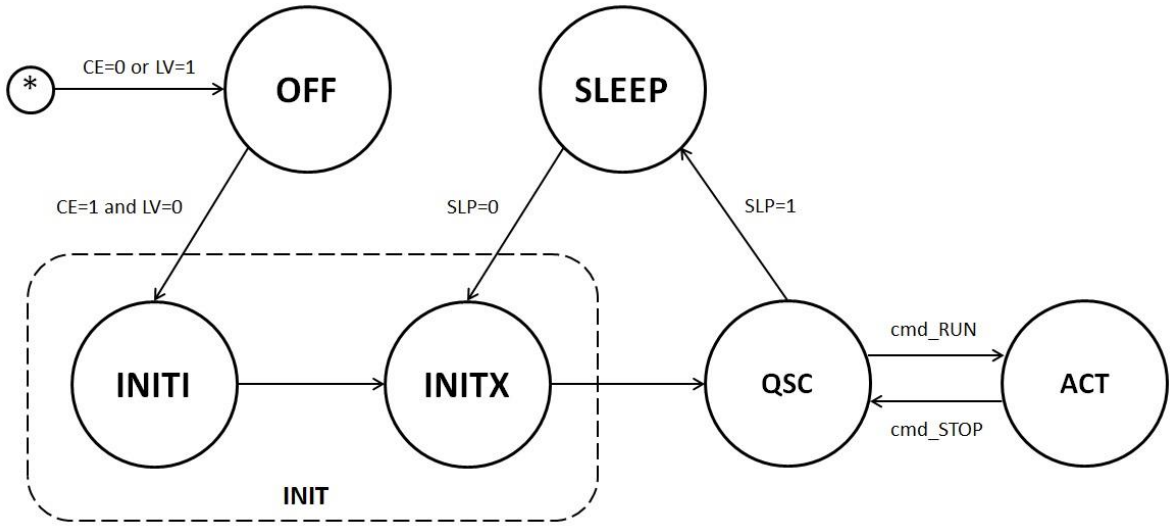


Figure 1. State Diagram

Protection Circuits

Thermal Shutdown: The KTX9602 has a built-in thermal shutdown function, which shuts down the device when junction temperature is over T_{SD}.

UVLO: The KTX9602 has a built-in UVLO function block for V_{CC} and V_{DD}. The hysteresis of V_{CC} UVLO threshold is V_{CCHYS}, and the one of V_{DD} is V_{DDHYS}. The device is locked out when V_{CC} is down to V_{CCUV}, or V_{DD} is down to V_{DDUV}; and woke up at V_{CC} is more than V_{CCUV}+V_{CCHYS} and VDD is more than V_{DDUV}+V_{DDHYS}.

Sleep Condition

The KTX9602 enters sleep condition to conserve energy, when **RUN_MODE** (0x03) is set as 0x00 and *PWM_AIN* (pin 11) input is <1.5% Duty ratio of Digital PWM signal or <0.03V Analog signal. When the device enters sleep, the motor engine stops driving. The I^2C interface is inactive, and any register data is maintained.

External Non-Volatile Memory

The KTX9602 uses external UNI/O Serial EEPROM – 11LC020 (256 x 8 bits) to store user-defined parameters. After reset, KTX9602 checks the logic level of SCIO – Pin 47 (Pulled-up internally). If it is High, it will autoload the parameters to the registers, from address 0x00 to 0xF9, that are stored in Serial EEPROM, which connects to Pin 47 – SCIO.

Then, the KTX9602 can operate at standalone mode, without I^2C communication. It uses Analog/PWM input command at PWM_AIN Pin 11.

KTX9602 Application Information

Status

There are several protection functions in KTX9602 that used to protect the devices and motor. The read-only **STATUTS** register shows the details with relative fault bit set.

All fault bits will be cleared after **STATUS** is reading through I^2C.

Register	Address	Bit							
		7	6	5	4	3	2	1	0
STATUS	**00h**	RNG	-	OT	GD_FLT2	GD_FLT1	NTC_FLT	VB_FLT	OC_FLT

RNG: Device Running

This is self-checking flag of KTX9602, when 0 is device failure; 1 is device running.

OT: Over Temperature

This bit is set to indicate KTX9602 in thermal shutdown status when junction temperature is over the spec. And *FLT* (pin 2) outputs low.

GD_FLT2: Gate Driver 2 Fault

This bit is set to indicate gate driver 2 fault warning when the input of *GD_FLT2* (pin 32) is low. This device turns off the driving PWM output and *FLT* (pin 2) outputs low.

GD_FLT1: Gate Driver 1 Fault

This bit is set to indicate gate driver 1 fault warning when the input of *GD_FLT1* (pin 24) is low. This device turns off the driving PWM output and *FLT* (pin 2) outputs low.

NTC_FLT: NTC High temparature Fault

This bit is set to indicate the NTC high temparature fault when the anlog input of *NTC/EXT* (pin 13) is lower than the set value of **NTCH_LMT** (0x9C). This device is shutdown and *FLT* (pin 2) outputs low when this bit is triggered, if the **PROT_EN** bit of **MODE_B** (0x92) is set.

VB_FLT: Under Voltage /Over Voltage Fault

This bit is set to indicate the UV/OV fault when the anlog input of *VM_SEN* (pin 12) is lower than the set value of **VBL_LMT** (0x9A) or higher than the set value of **VBH_LMT** (0x9B). This device is shutdown and *FLT* (pin 2) outputs low when this bit is triggered, if the **PROT_EN** bit of **MODE_B** (0x92) is set.

OC_FLT: Over Current Fault

This bit is set to indicate the over current fault when the sum of absolute **IU** (0x0e,0x0f), **IV** (0x10,0x11) and **IW** (0x12,0x13) value is over **IMAX** (0xDE,0xDF) for the set **OC_TIME** (0x2A) period. This device is shutdown and *FLT* (pin 2) outputs low when this bit is triggered.

Configuration

The KTX9602 is required to be configured before start motor driving.

The **CONFIG** (0x01) register is to configure the driving motor type and PWM output mode.

The **MODE** (0x02) register is to select the control functions.

The **PORT_EN** (0x0B) register is to configure the functions of IOs.

The **MODE_B** (0x92) register is to enable/disable protection and configure the control mode for PWM duty or Analog input command.

Register	Address	Bit							
		7	6	5	4	3	2	1	0
CONFIG	**01h**	-	-	FB_CFG	MOTOR_TYPE[1:0]		-	-	-

FB_CFG: PWM output driving mode for 6-wire motor only

The 6-wire full-bridge output is sinusoidal mode when this bit is cleared. The **VQ_MAX** (0x50,0x51) should be set less than 0.8227. In **VQ_MAX** (0x50,0x51) > 0.8227 condition, it will change to full-bridge SVM mode when **VQ** (0x80,0x81) is higher than 0.8227.

The 6-wire full-bridge output is SVM mode when this bit is set

MOTOR_TYPE[1:0]: Motor Type

00: 3-phase Full-Bridge (6-wire BLDC)

01: 2-phase Full-Bridge (Stepper motor)

10: 3-phase Half-Bridge (3-wire BLDC in Delta connection)

11: 3-phase Half-Bridge (3-wire BLDC in Star connection)

Register	Address	Bit							
		7	6	5	4	3	2	1	0
MODE	**02h**	IPD_MODE	DIR	RESTART_EN	OFFSET_C	INIT_R	-	EXT	FW_EN

IPD_MODE: Initial Position Detection mode

0: IPD Mode 0

1: IPD Mode 1

DIR: Motor rotating direction

0: Clockwise (CW)

1: Counter-Clockwise (CCW)

RESTART_EN: Restart Enable

To choose restart or stop motor driving when **FMAG** (0x96,0x97) is lower than set **FMAG_LOW** (0x6E,0x6F) value, that is used to determine whether the control works fine or not during motor control operation.

0: Disable – Stop

1: Enable – Restart

OFFSET_C: Shunt Sensor - ADC offset cancellation.

0: Disable

1: Enable

INIT_R: Initial motor resistance detection

Enable the detection of the initial motor resistance value when parking the motor to the specified angle. The calculated value will be storted at **R_STARTUP** (0x78,0x79).

0: Disable

1: Enable

EXT: Second-order close loop in external ADC input control

To select control mode for motor driving by targeting the external ADC input which replaces the speed/power target in second-order close loop on Field Oritented Control (FOC).

0: Disable

1: Enable

FW_EN: Look-up Table for Flux-Weakening control

To redefine the look-up table for flux-weakening control by replacing Maximum Torque Per Ampere (MTPA) feature.

0: Disable

1: Enable

Register	Address	Bit							
		7	6	5	4	3	2	1	0
PORT_EN	**0Bh**	DIR_EN	-	-	HALL_EN[2:0]			ON_EN	LED_EN

DIR_EN: Select the direction by the *DIR* pin. The direction is defined through the input logic level as: “CW” – “0”, “CCW” – “1” when it is enabled.

0: Disable

1: Enable

HALL_EN[2:0]: Select Hall sensor assistance function.

000: Disable

111: Enable

ON_EN: Select the Run/Stop by the *Run* pin. While it is enabled, it uses momentary push button to switch between STOP command, RUN command as the operation mode in **RUN_MODE** (0x03) register by changing the PWM_EN bit.

0: Disable

1: Enable

LED_EN: Output signal for LED indication on the RUN/STOP status.

0: Disable

1: Enable

Register	Address	Bit							
		7	6	5	4	3	2	1	0
MODE_B	**92h**	P_IPD	P_ISD	-	-	-	PROT_EN	PMODE[1:0]	

P_IPD: Initial Position Detection in PWM Duty/Analog input command

0: Disable

1: Enable

P_ISD: Initial Speed Detection in PWM Duty/Analog input command

0: Disable

1: Enable

PROT_EN: Fault Protection Enable

It is to enable the fault protection by stop motor driving when **NTC_FLT**, or **VB_FLT** is triggered.

0: Disable

1: Enable

P_MODE[1:0]: Control Mode for WM Duty/Analog Input command

00: VQ control

01: Torque control (FOC)

10: Speed control (FOC)

11: Power control (FOC)

Normalization

To simplify the calculation in the control algorithm, the current and voltage in KTX9602 are normalized to the range from -1.0 to 1.0.

The normalized current is presented by **I** with formula as below.

$$I = \frac{RESENSE}{VAD} * i \quad , i \textit{ is the phase current.}$$

Register	Address	Data				
AD_CONFIG	14h	AD_EN	AD_RANGE[1:0]			AD_SEL[2:0]
RSENSE	74h	RESENSE[-1:-8]				
	75h	RESENSE[-9:-16]				

The conversion of built-in ADC is signed (1 bit) with resolution of 11 bits. AD Range setting is to select the internal PGA with the input voltage range which is listed below:

AD RANGE[1:0]	Description
00	Input Voltage Range: (-1V to +1V)
01	Input Voltage Range: (-0.5V to +0.5V)
10	Input Voltage Range: (-0.25V to +0.25V)
11	Input Voltage Range: (-0.125V to +0.125V)

AD_EN: Turn on/off the Analog-Digital conversion on selected AD channel.

0: Off

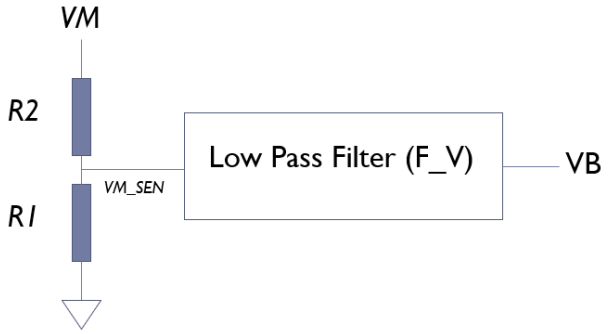
1: On

AD_SEL[2:0]: AD channel selection.

RSENSE[-1:-16]

The resistance of the shunt for current sensing.

The KTX9602 detects the bus voltage through the potentiometer circuit in the pin of *VM_SEN*. The range of ADC input is 0~2.0V.



Bus Voltage Sensing

The normalized bus voltage is presented by VB with formula as below.

$$VB = \frac{VM}{V\_RATIO},\ V\_RATIO = \frac{2(R2+R1)}{R1}$$

Register	Address	Data	
V_RATIO	54h	V_RATIO[9:2]	
	55h	V_RATIO[1:-6]	
VDC	72h	VDC[9:2]	
	73h	VDC[1:-6]	
VB	B6h	VB[-1:-8]	
	B7h	VB[-9:-16]	
KSCALE	B8h	0	KSCALE[13:7]
	B9h	KSCALE[6:-1]	
	Bah	KSCALE[-2:-9]	

V_RATIO[9:-6]

The ratio for bus voltage's normalization, which comes from the potentiometer circuit.

VDC[9:-6]

The bus voltage value is used for the calculation in the motor engine while the input of VM_SEN is lower than 0.125V.

VB[-1:-16] *Read-Only*

The ADC output for VM_SEN channel.

KSCALE[13:-9] *Read-Only*

The scaler is used for the calculation in the motor engine, which is defined by the following formula.

$$KSCALE = \frac{VAD}{RSENSE*VDC}$$, or $$KSCALE = \frac{VAD}{RSENSE*V\_RATIO*VB}$$

Safety Configuration

The KTX9602 offers several protection tasks through ADC sampling on phase current, bus voltage and NTC signal, including Over-Current protection, Over-Voltage protection, Under-Voltage protection, and NTC Over-Temperature protection.

Over-Current Protetion:

The KTX9602 detects the sum of IU, IV, IW absolution value each PWM cycle. The **OC_FLT** is triggered while the sum is more than **IMAX** (0xDE,0xDF) in the period as set **OC_TIME** (0x2A).

Register	Address	Data
OC_TIME	2Ah	OC_TIME[7:0]
IMAX	DEh	IMAX[1:-6]
	DFh	IMAX[-7:-14]
ITOTAL	9Dh	ITOTAL[2:-5]

OC_TIME[7:0]

The over current blanking time. The time interval equals to register value multiplied by 128 times PWM cycle time - 5.578mS (default).

IMAX[1:-14]

The maximum limit of over-current value.

ITOTAL[2:-5] *Read-Only*

The total current for all channels, which is defined by the following formula.

$$I_{Total} = |I_u| + |I_v| + |I_w|$$

Over-Voltage/Under-Voltage Protection

Register	Address	Data
VB0	1Ah	VB0[-1:-8]
VBL_LMT	9Ah	VBL_LMT[-1:-8]
VBH_LMT	9Bh	VBH_LMT[-1:-8]

VB0[-1:-8]

The normalized value of rated voltage, which is used as reference in the feed-forward loop.

VBL_LMT[-1:-8]

The minimum limit of bus voltage after the scaling.

VBH_LMT[-1:-8]

The maximum limit of bus voltage after the scaling.

NTC Over-Temperature Protection

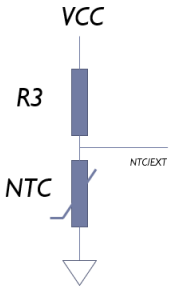
Register	Address	Data
NTCH_LMT	9Ch	NTCH_LMT[-1:-8]

NTCH_LMT[-1:-8]

The maximum limit of the input voltage in *NTC/EXT* pin.

The input voltage in *NTC/EXT* is defined as following formula.

$$V\_NTC = VCC * \frac{RNTC}{R3+RNTC}$$



The NTC over-temperature fault is triggered by the input voltage of *NTC/EXT*

Is less than **NTCH_LMT** (0x9C) value.

PWM Output Configuration

The KTX9602 offers the configuration on the dead-time, maximum High-side duty ratio and PWM frequency to match given MOSFETs or IGBT operation conditions.

Register	Address	Data
ONOFF_TIME	04h	ONOFF_TIME[7:0]
OFF_WIDTH	05h	OFF_WIDTH[7:0]
PWM_PERIOD	06h	PWM_PERIOD[7:0]

ONOFF_TIME[7:0]

The dead-time for the transition between High-side and Low-side PWM output. The time interval equals to register value multiplied by 21.28nS.

OFF_WIDTH[7:0]

The minimum Low-side ON time, which is as High-side bootstrap capacitor charging time. The time interval equals to register value multiplied by 21.28nS.

PWM_PERIOD[7:0]

To configure the PWM output frequency, which equals to 734.375KHz divided by register value.

Motor Speed Parameter

In the control algorithm, KTX9602 defines the motor speed (ω) as motor angle advanced per PWM cycle. This internal representation differs from general motor speed (RPM) definition of number of rotations per minute.

$$\omega = RPM * \frac{SPEED\_CONSTANT}{FREQ} * POLE\_PAIR$$

And it is allowed to amend the speed calculation by inputting the user value.

Register	Address	Data
POLE_PAIR	61h	POLE_PAIR[7:0]
FREQ	62h	FREQ[15:8]
	63h	FREQ[7:0]
SPEED_CONSTANT	58h	SPEED_CONSTANT[13:6]
	59h	SPEED_CONSTANT[5:-2]

POLE_PAIR[7:0]

The pole-pairs number of the motor.

FREQ[15:0]

The PWM frequency is used for the internal calculation in the control algorithm, especially for rotating speed and inductance related part.

SPEED_CONSTANT[13:-2]

Coefficient for internal speed calculation.

Angle Adjustment

Considering the inductive effect of the motor's windings, it is often desirable to control the drive state of the motor so that the phase current of motor is aligned with the BEMF voltage of the motor. The KTX9602 provides the configuration for controlling the timing adjustment between the driving voltage and phase current.

Register	Address	Data	
TIME_ADJ	7Eh	Sign	TIME_ADJ[1:-5]
	7Fh	TIME_ADJ[-6:-13]	
ANGLE_ADJ	BCh	Sign	ANGLE_ADJ[13:7]
	BDh	ANGLE_ADJ[6:-1]	

TIME_ADJ±[1:-13]

The ratio of time adjustment .

ANGLE_ADJ±[13:-1] *Read-Only*

The adjusted angle, which is defined by the following formula.

$$Adj\ Angle = TIM\_ADJ * \omega$$

Digital High/Low Pass Filter

There are 1 first-order digital HPF and 4 first-order digital LPF that are used in the motor engine.

As below, the formula of LPF is Eq(1), and the formula of HPF is Eq(2).

y(n) = y(n-1) + a * (x(n)-y(n-1)) Eq(1)

y(n) = x(n) – LPF(x(n)) Eq(2)

a: Coefficient

Register	Address	Data
F_A	64h	F_A[-1:-8]
	65h	F_A[-9:-16]
F_B	66h	F_B[-1:-8]
	67h	F_B[-9:-16]
F_C	68h	F_C[-1:-8]
	69h	F_C[-9:-16]
F_V	70h	F_V[-1:-8]
	71h	F_V[-9:-16]
F_DQ	F2h	F_DQ[-1:-8]
	F3h	F_DQ[-9:-16]

F_A[-1:-16]

The coefficient of first-order HPF for Position/Angle Estimation.

F_B[-1:-16]

The coefficient of first-order LPF for Position/Angle Estimation.

F_C[-1:-16]

The coefficient of first-order LPF for Speed/Power Estimation.

F_V[-1:-16]

The coefficient of first-order LPF which is used in VB Measuring.

F_DQ[-1:-16]

The coefficient of first-order LPF for VQ/VD calculation when Flux-weakening function is enabled.

Motor Control

The KTX9602 offers 2 types of command to control the motor driving: one is adjusting either the PWM Duty or Analog voltage at *PWM_AIN* (pin 11), the other is writing the command directly to **RUN_MODE** (0x03) through the I²C serial port.

Motor Start Sequence

Figure 2 shows the motor start sequence.

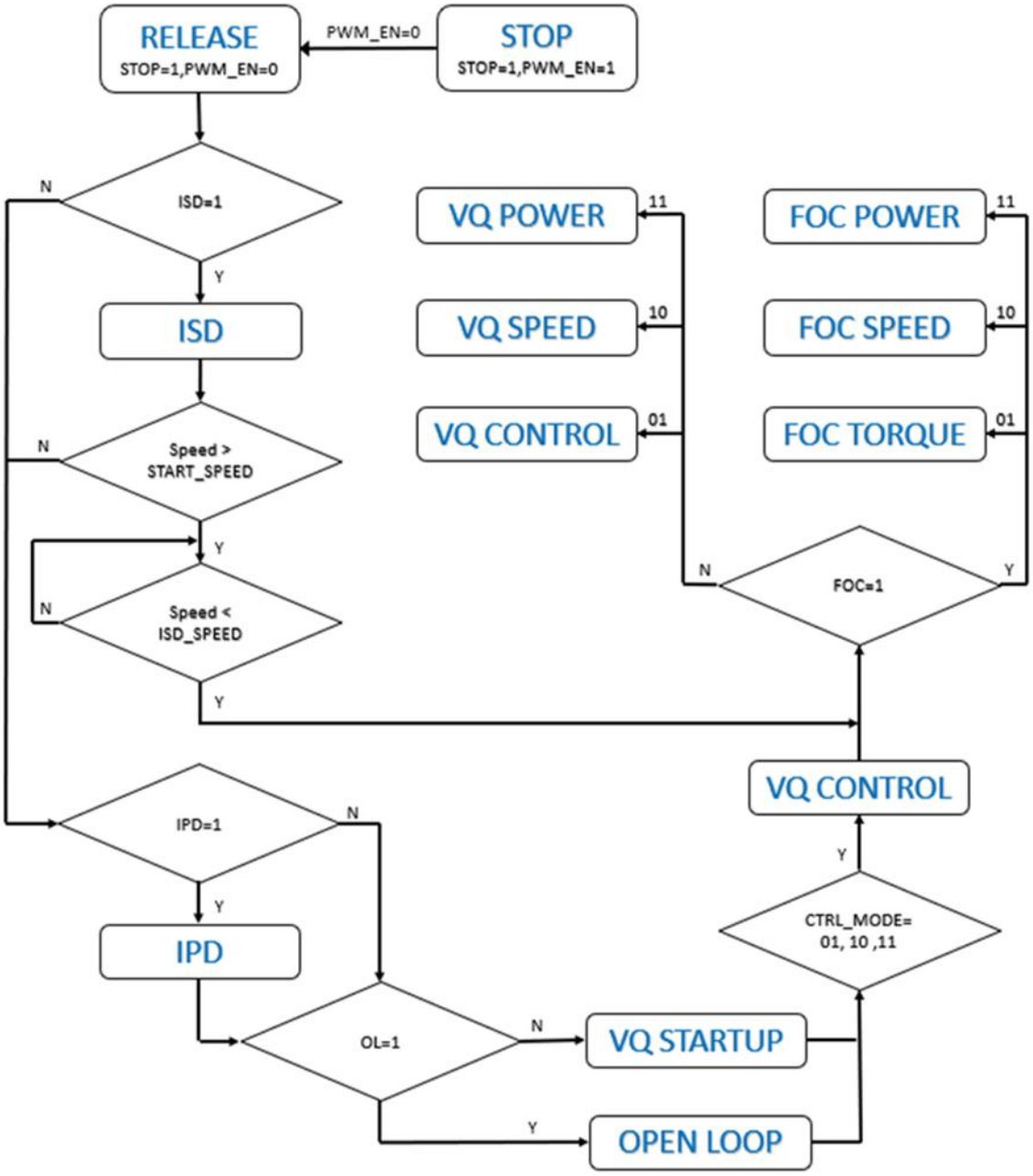


Figure 2. Motor Start Sequence

Motor Operation Mode

RELEASE: Turn off all MOSFETs
STOP: Turn off all High side MOSFETs and Turn on all Low side MOSFETs
PARKING: Align the motor by injecting DC current through a specific phase pattern which is based on the configured angle.
OPEN LOOP: A simple Volts/Hz control to accelerate the motor from still.
IPD (Initial Position Detection): Detect the motor initial position when the motor is still.
ISD (Initial Speed Detection): Detect the motor initial speed before driving the motor.
VQ STARTUP: A specific close-loop type startup method for achieving reliable and fast startup even in variable torque condition.
VQ CONTROL: A semi-closed-loop system, which provides fast torque-response control.
TORQUE CONTROL (Field Oriented Control): A first-order closed-loop current control, which is provides good control capability over the full torque ranges.
SPEED CONTROL: A second-order closed-loop speed control, which is based on Field Oriented Control or Direct VQ Control.
POWER CONTROL: A second-order closed-loop power control, which is based on Field Oriented Control or Direct VQ control.

The KTX9602 configures the operation mode through the register **RUN_MODE** (0x03). Table 1 lists the commonly used modes.

Table 1. Commonly Used Modes

Operation Mode	RUN_MODE (0x03)	Data						
		IPD	ISD	STOP	FOC	OL	CTRL_MODE[1:0]	PWM_EN
P_MODE Enable	00h	0	0	0	0	0	00	0
RELEASE	20h	0	0	1	0	0	00	0
STOP	21h	0	0	1	0	0	00	1
PARKING	29h	0	0	1	0	1	00	1
OPEN LOOP	09h	0	0	0	0	1	00	1
VQ STARTUP	01h	0	0	0	0	0	00	1
ISD>IPD>VQ STARTUP>VQ CONTROL	C3h	1	1	0	0	0	01	1
ISD>VQ STARTUP>VQ CONTRL>VQ SPEED	45h	0	1	0	0	0	10	1
ISD>VQ STARTUP>VQ CONTROL>FOC TORQUE	53h	0	1	0	1	0	01	1
VQ STARTUP>VQ CONTROL>FOC TORQUE>FOC SPEED	15h	0	0	0	1	0	10	1
ISD>VQ STARTUP>VQ CONTROL>FOC TORQUE>FOC POWER	57h	0	1	0	1	0	11	1
ISD>IPD>OPEN LOOP>VQ CONTROL>FOC TORQUE	DBh	1	1	0	1	1	01	1
ISD>OPEN LOOP>VQ CONTROL>FOC TORQUE>FOC POWER	5Fh	0	1	0	1	1	11	1
OPEN LOOP>VQ CONTRL>FOC TORQUE>FOC SPEED	1Dh	0	0	0	1	1	10	1

Details:

Parking
This function is to align a motor at the specified position by injecting DC current through a particular phase pattern which calculated from the user defined angle.

Register	Address	Data
PARK_PWM	1Fh	PARK_PWM[-1:-8]
THETA	40h	THETA[14:7]
	41h	THETA[6:-1]

PARK_PWM[-1:-8]

PWM output amplitude in 1.0 scaler for parking, Maximum value is 0.996, default value is 0.125.

THETA[14:-1]

Theta (electrical angle) setting for parking/running.

$$Angle = \frac{THETA}{32768} * 360^{\circ}$$

IPD (Initial Position Detection)
This function can be used in applications where reverse rotation of the motor is not acceptable. It uses the inductive sense method to determine the initial position of the motor when this function is enabled. Because it works by pulsing current to the windings of motor, it generates acoustics, which should be considered when determining the best start method for a particular application.

Register	Address	Data
PARK_PWM	1Fh	PARK_PWM[-1:-8]
IPD_TIME	40h	IPD_TIME[7:0]
OFF_TIME	41h	OFF_TIME[7:0]

There are 2 IPD Mode, which is selected by **IPD** bit in **MODE** (0x02).
IPD Mode 0, Angle 0 >> 180 >> 30 >> 210 >> 60 >> 240 >> 90 >> 270 >> 120 >> 300 >> 150 >> 330. It will apply the pulse output with setting parking PWM amplitude, following the above angle sequence.
IPD Mode 1, Angle 0 >> 30 >> 60 >> 90 >> 120 >> 150 >> 180 >> 210 >> 240 >> 270 >> 300 >> 330. It will run the pulse injecting operation twice with setting parking PWM amplitude, following the above angle sequence.

PARK_PWM[-1:-8]

PWM output amplitude in 1.0 scaler for parking, Maximum value is 0.996, default value is 0.125.

IPD_TIME[7:0]

Duration time of parking pulse applied to the motor in each angle. The length of time equals to the register value multiplied by PWM cycle time - 43.57uS (default).

OFF_TIME[7:0]

Resting time for releasing inductance current before next detection pulse. The length of time equals to the register value multiplied by 64 times PWM cycle time - 2.789mS (default).

ISD (*Initial Speed Detection*)
This function is used to detect the initial speed. If the detected speed in first stage is lower than **START_SPEED** (0x42,0x43), it will end this detect function, and treats the motor as it is stationary. Otherwise, it detects the higher speed limit in second stage. If the detected speed is lower than **ISD_SPEED** (0xF6,0xF7), it will transit directly into the close loop running state without needing to run through the start-up procedure. Otherwise, it will repeat the second process until the speed decelerates to defined speed range, then transit to close loop running state.

Register	Address	Data
ISD_TIME1	20h	ISD_TIME1[7:0]
ISD_TIME2	21h	ISD_TIME2[7:0]
START_SPEED	42h	START_SPEED[15:8]
	43h	START_SPEED[7:0]
ISD_SPEED	F6h	ISD_SPEED[15:8]
	F7h	ISD_SPEED[7:0]

ISD_TIME1[-1:-8]

Duration time for the first round – low speed detection. The length of time equals to the register value multiplied by 256 times PWM cycle time - 11.155ms (default).

ISD_TIME2[-1:-8]

Duration time for the second round – high speed detection. The length of time equals to the register value multiplied by 256 times PWM cycle time - 11.155ms (default).

START_SPEED[15:0]

Lower speed limit in ISD speed range.

ISD_SPEED[15:0]

Higher speed limit in ISD speed range.

Open Loop (Voltage/Hertz Control)

This function is to accelerate or decelerate the motor by applying the voltage determined by the relative VQ equation, from **START_SPEED** (0x42,0x43) to **END_SPEED** (0x44,0x45).

Register	Address	Data	
OL_TIME	23h	OL_TIME[7:0]	
START_SPEED	42h	START_SPEED[15:8]	
	43h	START_SPEED[7:0]	
END_SPEED	44h	END_SPEED[15:8]	
	45h	END_SPEED[7:0]	
A1	46h	Sign	A1[7:1]
	47h	A1[0:-7]	
A2	48h	Sign	A2[3:-3]
	49h	A2[-4:-11]	
START_VQ	4Ah	START_VQ[-1:-8]	
	4Bh	START_VQ[-9:-16]	
KINV	4Ch	0	KINV[13:7]
	4Dh	KINV[6:-1]	
	4Eh	KINV[-2:-9]	
	4Fh	KINV[-10:-17]	

OL_TIME[-1:-8]

Time interval for each step of acceleration or deceleration. The length of time equals to the register value multiplied by 256 times PWM cycle time - 11.155ms (default).

START_SPEED[15:0]

Starting speed in this acceleration/deceleration operation.

END_SPEED[15:0]

Target speed in this acceleration/deceleration operation.

A1±[7:-7]

First order accelerate/decelerate rate in this acceleration/deceleration operation.

A2±[3:-11]

Second order accelerate/decelerate rate in this acceleration/deceleration operation.

START_VQ[-1:-16]

Starting VQ in this acceleration/deceleration operation.

KINV[13:-17]

BEMF parameter, used for the calculation of VQ in Open Loop operation.

The open loop speed $Speed_{OL}$ is defined by the following equation.

$$Speed_{OL} = START\_SPEED + A1 \times t + \frac{1}{2}(A2 \times t^2), Where\ t\ is\ number\ of\ LOCK_{TIME}$$

During the acceleration/deceleration, **VQ** will be updated from **START_VQ** (0x4A,0x4B) by the following equation.

$$VQ = START\_VQ + \frac{\omega ol}{KINV}$$

$$KINV = 60 * VDC * \frac{SPEED\_CONSTANT}{FREQ} * \frac{Frequency\_BEMF}{VPEAK\_BEMF}$$

Frequency_BEMF: The Frequency of phase's Back EMF

VPEAK_BEMF: The Peak Voltage of phase's Back EMF

Furthermore, the **VQ** will be bounded in the range from **VQ_MIN** (0x52,0x53) to **VQ_MAX** (0x50,0x51)

$$VQ\_MIN \leq VQ \leq VQM\_START \leq VQ\_MAX$$

VQ Startup

In this close loop startup, the motor is driven with specific angle for certain period. And the motor will be secured to rotate at right direction even there is torque change by observing the flux magnitude information.

Register	Address	Data
STARTUP_TIME	22h	STARTUP_TIME[7:0]
OL_TIME	23h	OL_TIME[7:0]
START_SPEED	42h	START_SPEED[15:8]
	43h	START_SPEED[7:0]
START_VQ	4Ah	START_VQ[-1:-8]
	4Bh	START_VQ[-9:-16]
R_STARTUP	78h	R_STARTUP[5:-2]
	79h	R_STARTUP[-3:-10]
L_STARTUP	7Ah	L_STARTUP[4:-3]
	7Bh	L_STARTUP[-4:-11]
	7Ch	L_STARTUP[-12:-19]
MIN_DTHETA	7Dh	MIN_DTHETA[13:6]

STARTUP_TIME[-1:-8]

Time interval for each step driving, which has the same estimated angle. The length of time equals to the register value multiplied by 9 times PWM cycle time - 392.17us (default).

OL_TIME[-1:-8]

Time interval of acceleration in open loop before the VQ startup operation. The length of time equals to the register value multiplied by 256 times PWM cycle time - 11.155ms (default). This open loop may be running for a short period to have smooth rotating from still. It can be set as 0 to run the VQ startup directly.

START_SPEED[15:0]

The running speed of open loop before the VQ startup operation.

START_VQ[-1:-16]

It is the fixed VQ used in this startup operation.

R_STARTUP[5:-10]

The phase's resistance in the VQ startup operation, which is used for flux and angle estimation.

L_STARTUP[4:-19]

The phase's inductance in the VQ startup operation, which is used for flux and angle estimation.

MIN_DTHETA[13:6]

Minimum angle change between steps in this operation.

VQ Control

In this close loop operation, the driver is controlled based on VQ as the target. It continuously measures the motor current and uses this information to control the drive state of the motor with dedicated motor engine.

Register	Address	Data
LOCK_TIME	1Eh	LOCK_TIME[7:0]
VQ_TIME	24h	VQ_TIME[7:0]
R_VQ	96h	R_VQ[5:-2]
	97h	R_VQ[-3:-10]
L_VQ	08h	L_VQ[4:-3]
	09h	L_VQ[-4:-11]
	0Ah	L_VQ[-12:-19]
DELTA_VQ	6Ah	DELTA_VQ[-1:-8]
	6Bh	DELTA_VQ[-9:-16]
TARGET_VQ	6Ch	TARGET_VQ[-1:-8]
	6Dh	TARGET_VQ[-9:-16]
FMAG_LOW	6Eh	FMAG_LOW[6:-1]
	6Fh	FMAGE_LOW[-2:-9]
FMAG	96h	FMAG[13:6]
	97h	FMAG[5:-2]

LOCK_TIME[-1:-8]

Time interval of VQ Startup before transiting to VQ control operation. The length of time equals to the register value multiplied by 256 times PWM cycle time - 11.155ms (default).

VQ_TIME[-1:-8]

Time interval of each step for VQ ramping up in VQ control. The length of time equals to the register value multiplied by 256 times PWM cycle time – 11.155ms (default).

R_VQ[5:-10]

The phase’s resistance in the VQ control operation, which is used for flux and angle estimation.

L_VQ[4:-19]

The phase’s inductance in the VQ control operation, which is used for flux and angle estimation.

DELTA_VQ[-1:-16]

The stepping VQ which is to be increased from **START_VQ** (0x4A,0x4B) to **TARGET_VQ** (0x6C,6D).

TARGET_VQ[-1:-16]

The goal of VQ in this VQ Control operation.

FMAG_LOW[6:-9]

The lowest flux magnitude value for the detection of normal operation. If it detects that **FMAG** (0x96,0x97) is lower than this set value, it means the abnormal operation, and the motor will be stopped or re-start the motor control through start sequence without ISD, which is selected by the **RESTART_EN** bit in **MODE** (0x02).

FMAG[13:-2] *Read-Only*

The current flux magnitude.

During the operation, VQ will increase up to **TARGET_VQ** from **START_VQ** by the following equation.

$$VQ = START\_VQ + (DELTA\_VQ) * t, Where\ t\ is\ number\ of\ VQ\_TIME$$

Noted: The final VQ value in this operation is limited by "VQM_START", which means if "TARGET_VQ" is larger than "VQM_START", the VQM_START will be the actural TARGET_VQ.

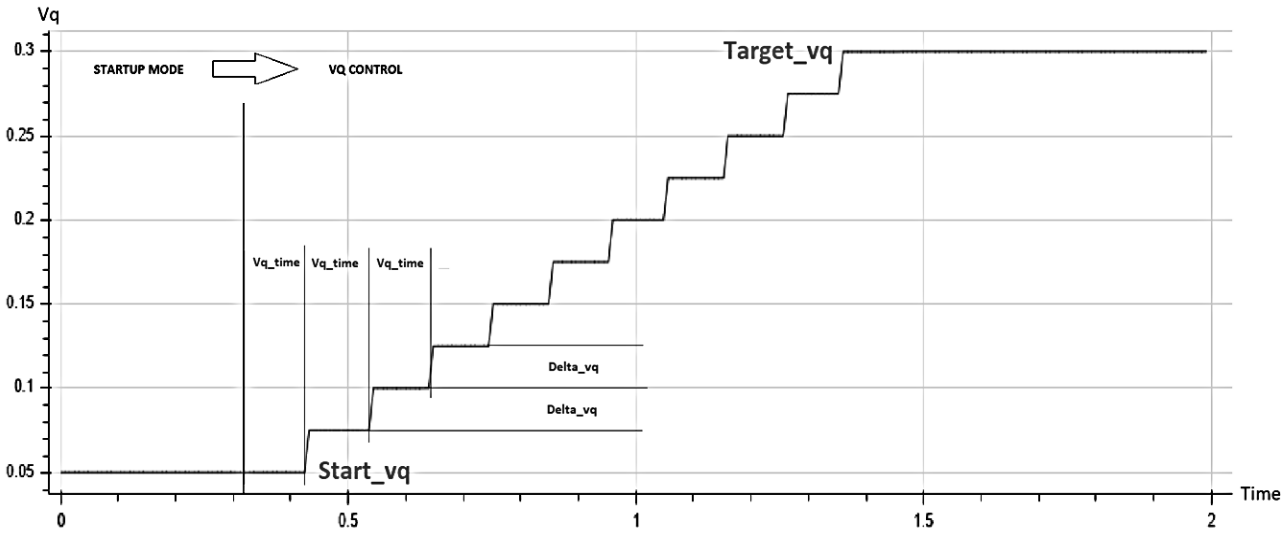


Figure 2. The Example of VQ increment in VQ Control Operation

FOC (Field Oriented Control) Torque Control

In FOC, the torque in the synchronous machine is a vector cross product of the stator field or current vector and rotor magnetic field vector. To get maximum torque with given stator current, the stator current vector and rotor magnetic field vector should be orthogonal, which means it is to keep the angle at 90° through the position and speed estimation by measuring the three-phase stator currents.

It provides the constant torque control as the first order control loop, as shown below in Figure 3. And the motor torque is defined by the following equation.

$torque_{Motor} = K_{torque} \times I_q$, where K_{torque} is torque constant of motor, I_q is quadrature/motor current.

Therefore, by controlling IQ to certain set value "TARGET_IQ", we can control the motor torque. In practice, we further control "TARGET_ID" to minimize power loss, especially for interior permanent-magnet synchronous motor (IPMSM).

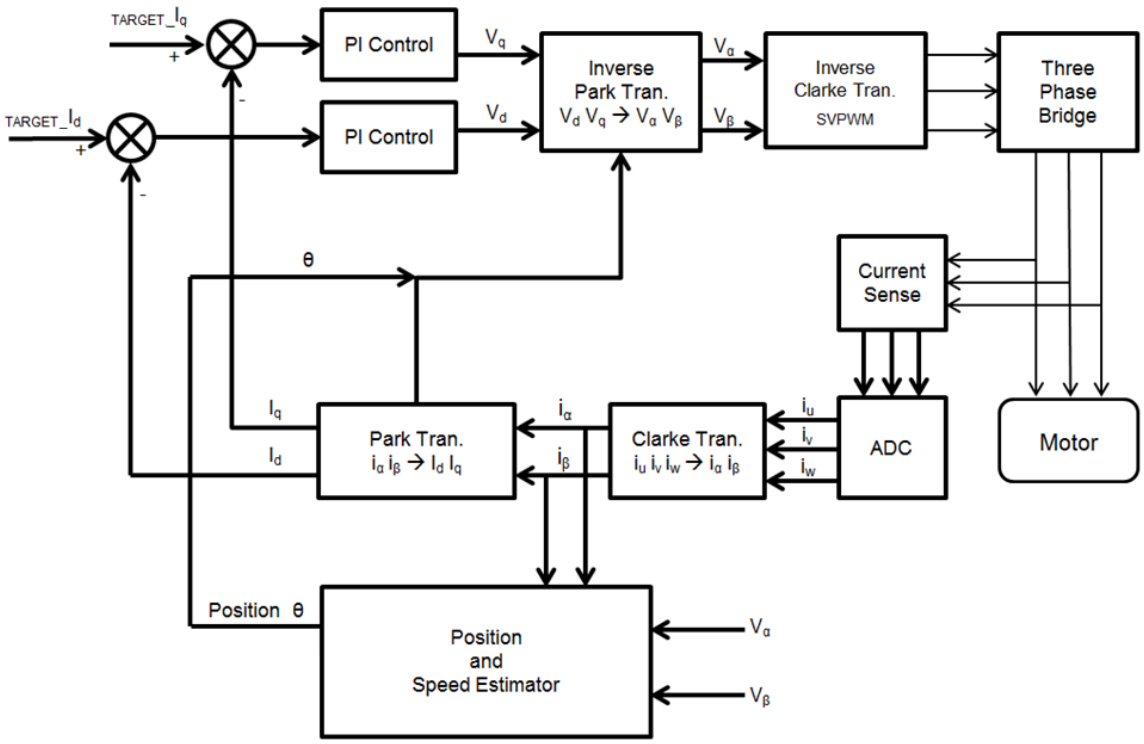


Figure 3. The Block Diagram of Torque Control in FOC Operation

Register	Address	Data
R_FOC	5Ch	R_FOC[5:-2]
	5Dh	R_FOC[-3:-10]
L_FOC	5Eh	L_FOC[4:-3]
	5Fh	L_FOC[-4:-11]
	60h	L_FOC[-12:-19]
VQM_START	2Bh	VQM_START[-1:-8]
VQM_RAMP	2Ch	VQM_RAMP[-1:-8]
VQM_TIME	2Dh	VQM_TIME[0:7]
VQ_MAX	50h	VQ_MAX[-1:-8]
	51h	VQ_MAX[-9:-16]
VQ_MIN	52h	Sign | VQ_MIN[-1:-7]
	53h	VQ_MIN[-8:-15]
TARGET_IQ	C0h	Sign | TARGET_IQ[-1:-7]
	C1h	TARGET_IQ[-8:-15]
KP_IQ	C2h	KP_IQ[1:-6]
	C3h	KP_IQ[-7:-14]
KI_IQ	C4h	KI_IQ[1:-6]
	C5h	KI_IQ[-7:-14]
KE_IQ	C6h	KE_IQ[1:-6]
	C7h	KE_IQ[-7:-14]

To enhance the stability during the FOC constant torque control loop, the maximum of VQ value will be limited by **VQ_MAX** (0x50,0x51). Also to prevent the overshoot while just entering into the FOC operation, the allowed VQ value will start from **VQM_START** (0x2B) by the following equation.

$$VQ\_MAX = VQM\_START + (VQM\_RAMP) * t, Where\ t\ is\ number\ of\ VQM\_TIME$$

R_FOC[5:-10]

The phase's resistance in the FOC operation, which is used for flux and angle estimation.

L_FOC[4:-19]

The phase's inductance in the FOC operation, which is used for flux and angle estimation.

VQM_START[-1:-8]

The initial maximum VQ just when transiting to FOC operation.

VQM_RAMP[-1:-8]

The stepping maximum VQ as the above equation.

VQM_TIME[7:0]

Time interval of each step for maximum VQ rising in FOC. The length of time equals to the register value multiplied by 256 times PWM cycle time – 11.155ms (default).

VQ_MAX[-1:-16]

The final maximum VQ limit used in current/torque regulator.

VQ_MIN±[-1:-15]

The minimum VQ limit used in current/torque regulator.

TARGET_IQ±[-1:-15]

The torque command which is presented as IQ value used in current/torque regulator.

KP_IQ[1:-14]

The proportional gain of PI control for IQ in current/torque regulator.

KI_IQ[1:-14]

The integral gain of PI control for IQ in current/torque regulator.

KE_IQ[1:-14]

The sum of error of PI control for IQ in current/torque regulator.

Register	Address	Data	
VD_MAX	C8h	VQ_MAX[-1:-8]	
	C9h	VQ_MAX[-9:-16]	
VD_MIN	CAh	Sign	VQ_MIN[-1:-7]
	CBh	VQ_MIN[-8:-15]	
TARGET_ID	DCh	Sign	TARGET_IQ[-1:-7]
	DDh	TARGET_IQ[-8:-15]	
KP_ID	CCh	KP_IQ[1:-6]	
	CDh	KP_IQ[-7:-14]	
KI_ID	CEh	KI_IQ[1:-6]	
	CFh	KI_IQ[-7:-14]	
KE_ID	D0h	KE_IQ[1:-6]	
	D1h	KE_IQ[-7:-14]	

VD_MAX[-1:-16]

The maximum VD limit used in current/torque regulator.

VD_MIN±[-1:-15]

The minimum VD limit used in current/torque regulator.

TARGET_ID±[-1:-15]

The flux command which is presented as ID value used in current/torque regulator.

KP_ID[1:-14]

The proportional gain of PI control for ID in current/torque regulator.

KI_ID[1:-14]

The integral gain of PI control for ID in current/torque regulator.

KE_ID[1:-14]

The sum of error of PI control for ID in current/torque regulator.

Speed/Power Control

The speed or power control is a second order closed loop control, which is based on Field Oriented Control. The block diagram is shown below as Figure 4.

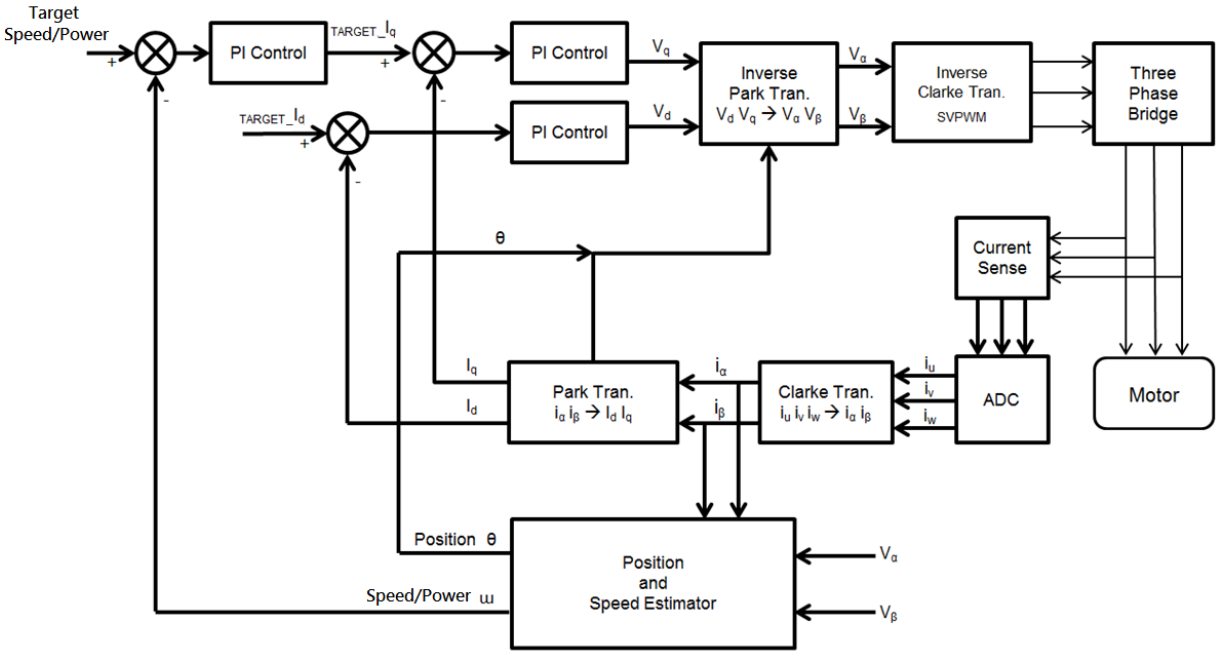


Figure 4. The Block Diagram of Speed/Power Control, which is Based on FOC

Since the speed/ power control are using the same PI regulator, so the registers shown in below table are use in common.

Register	Address	Data
FT_TIME	25h	FT_TIME[7:0]
SP_TIME	26h	SP_TIME[7:0]
MAX_ERR	76h	MAX_ERR[7:0]
	77h	MAX_ERR[-1:-8]
IQ_MAX	D2h	IQ_MAX[-1:-8]
	D3h	IQ_MAX[-9:-16]
IQ_MIN	D4h	Sign | IQ_MIN[-1:-7]
	D5h	IQ_MIN[-8:-15]
KP_SP	D6h	KP_SP[1:-6]
	D7h	KP_SP[-7:-14]
KI_SP	D8h	KI_SP[1:-6]
	D9h	KI_SP[-7:-14]
KE_SP	DAh	KE_SP[1:-6]
	DBh	KE_SP[-7:-14]
TARGET_IQ2	8Eh	Sign | TARGET_IQ2[-1:-7]
	8Fh	TARGET_IQ2[-8:-15]

FT_TIME[7:0]

Time duration of torque/current loop control before moving to second-order speed/power control loop.

SP_TIME[7:0]

Time interval of the PI control in second-order speed/power regulator.

MAX_ERR[7:0]

The maximum limit of error in the PI control of second-order speed/power regulator.

IQ_MAX[-1:-16]

The maximum IQ limit used in second-order speed/power regulator.

IQ_MIN±[-1:-15]

The minimum IQ limit used in second-order speed/power regulator.

KP_SP[1:-14]

The proportional gain of PI control for speed/power in second-order speed/power regulator.

KI_SP[1:-14]

The integral gain of PI control for speed/power in second-order speed/power regulator.

KE_SP[1:-14]

The sum of error of PI control for speed/power in second-order speed/power regulator.

TARGET_IQ2±[-1:-15] *Read-Only*

The Target IQ value which is used as the input to current/torque regulator. It comes from second-order speed/power regulator.

Register	Address	Data	
TARGET_SPEED	5Ah	TARGET_SPEED[15:8]	
	5Bh	TARGET_SPEED[7:0]	
TARGET_POWER	56h	TARGET_POWER[-2:-9] or [-3:-10] (P_MODE)	
	57h	TARGET_POWER[-10:-17] or [-11:-18] (P_MODE)	
F_SPEED	A2h	Sign	F_SPEED[15:9]
	A3h	F_SPEED[8:1]	
POWER_LPF	AEh	Sign	POWER_LPF[-2:-8] or [-3:-10] (P_MODE)
	AFh	POWER_LPF[-9:-16] or [-11:-17] (P_MODE)	

TARGET_SPEED[15:0]

The speed (rpm) command which is used in second-order speed/power regulator.

TARGET_POWER[-2:-17] or [-3:-18] (P_MODE)

The power command which is in second-order speed/power regulator. The power value is scaled to 0~0.5 (normal) or 0~0.25 (P_MODE).

F_SPEED±[15:1] *Read-Only*

The speed (rpm) which is calculated in position & speed estimation.

POWER_LPF±[-2:-16] or ±[-3:-17] (P_MODE) *Read-Only*

The power value which is output from power estimation.

Hall Sensor Assistant

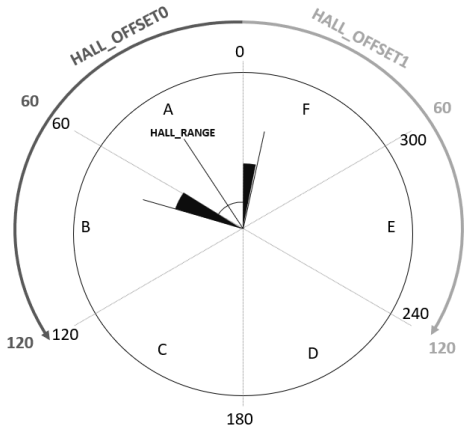
In case that 3 hall sensors are installed in motor, the KTX9602 can enable hall sensor assistant in all motor driving mode.

The 3 hall sensors will divide the motor angle into 6 sectors of 60° .HALL3/2/1 are input pins of KTX9602.

Sector	Hall3/2/1
A	001
B	101
C	100
D	110
E	010
F	011

Direction = 0

Direction = 1



To support diverse hall sensor configurations, it uses HALL_OFFSET0/1 for the sector adjustment in both CW/CCW direction.

In the motor engine, KTX9602 will determine the electrical angle by the position/angle estimator. To facilitate the operation and smooth transition between each angle sector, it is allowed to be out of the angle bounded by 60° angle sector, which is defined at **HALL_RANGE** (0x2E).

Register	Address	Data
HALL_RANGE	2Eh	HALL_RANGE[7:0]
HALL_OFFSET0	F8h	HALL_OFFSET0[7:0]
HALL_OFFSET1	F9h	HALL_OFFSET1[7:0]

HALL_RANGE[7:0]

The allowable hall range for each angle sector.

$$Hall\ Range\ = \frac{HALL\_RANGE}{255} * 360^{\circ}$$

HALL_OFFSET0[7:0]

The hall angle offset for Clockwise direction.

HALL_OFFSET1[7:0]

The hall angle offset for Counterclockwise direction.

$$Hall\ Offset\ = \frac{HALL\_OFFSET}{255} * 360^{\circ}$$

I²C Registers

I²C Slave Address

Options	7-Bit Address	Write Address	Read Address	Bits 7 6 5 4 3 2 1 0
KTX9602	0x78	0xF0	0xF1	1 1 1 1 0 0 0 *R/W*

I²C Register Map

Hex Address	Name	Type	Access	Default Reset	B7	B6	B5	B4	B3	B2	B1	B0
0x00	STATUS	Status	R	1000 0000	RNG	-	OT	GD_FLT2	GD_FLT1	NTC_FLT	VB_FLT	OC_FLT
0x01	CONFIG	Config	R/W	0000 0000	-	-	FB_CFG	MOTOR_TYPE[1:0]		-	-	-
0x02	MODE	Config	R/W	0011 0000	IPD_MODE	DIR	RESTART_EN	OFFSET_C	INIT_R	-	EXT	FW_EN
0x03	RUN_MODE	Config	R/W	0010 0000	IPD	ISD	STOP	FOC	OL	CTRL_MODE[2:0]		PWM_EN
0x04	ONOFF_TIME	Config	R/W	0000 1000	ONOFF_TIME[7:0]							
0x05	OFF_WIDTH	Config	R/W	0100 0000	OFF_WIDTH[7:0]							
0x06	PWM_PERIOD	Config	R/W	0010 0000	PWM_PERIOD[7:0]							
0x07	DELTA_ID	Config	R/W	0000 0000	DELTA_ID[-3:-10]							
0x08	L_VQ	Config	R/W	0000 0000	L_VQ[4:-3]							
0x09				0000 0010	L_VQ[-4:-11]							
0x0A				0001 1000	L_VQ[-12:-19]							
0x0B	PORT_EN	Config	R/W	0000 0000	DIR_EN			HALL_EN[2:0]			ON_EN	LED_EN
0x0E	IU	Data	R	0000 0000	Sign	IU[-1:-7]						
0x0F				0000 0000	IU[-8:-15]							
0x10	IV	Data	R	0000 0000	Sign	IV[-1:-7]						
0x11				0000 0000	IV[-8:-15]							
0x12	IW	Data	R	0000 0000	Sign	IW[-1:-7]						
0x13				0000 0000	IW[-8:-15]							
0x14	AD_CONFIG	Config	R/W	01100101	AD_EN	AD_RANGE[1:0]		-	-	AD_SEL[2:0]		
0x15	TARGETID_MAX	Config	R/W	1000 0000	TARGETID_MAX[-1:-8]							
0x16	VS2_MAX2	Config	R/W	1111 1111	VS2_MAX2[-1:-8]							
0x17	VS2_MAX1	Config	R/W	1111 1111	VS2_MAX1[-1:-8]							
0x18	VS2_MAX0	Config	R/W	0000 0000	VS2_MAX0[-1:-8]							
0x19	IS2_MAX	Config	R/W	1111 1111	IS2_MAX[-1:-8]							
0x1A	VB0	Config	R/W	1000 0000	VB0[-1:-8]							
0x1E	LOCK_TIME	Config	R/W	0001 0000	LOCK_TIME[7:0]							
0x1F	PARK_PWM	Config	R/W	0001 0000	PARK_PWM[-1:-8]							

Hex Address	Name	Type	Access	Default Reset	B7	B6	B5	B4	B3	B2	B1	B0
0x20	ISD_TIME1	Config	R/W	0000 1010	ISD_TIME1[7:0]							
0x21	ISD_TIME2	Config	R/W	0010 0000	ISD_TIME2[7:0]							
0x22	STARTUP_TIME	Config	R/W	0001 0000	STARTUP_TIME[7:0]							
0x23	OL_TIME	Config	R/W	0001 0000	OL_TIME[7:0]							
0x24	VQ_TIME	Config	R/W	0001 0000	VQ_TIME[7:0]							
0x25	FT_TIME	Config	R/W	0001 0000	FT_TIME[7:0]							
0x26	SP_TIME	Config	R/W	0001 0000	SP_TIME[7:0]							
0x27	IPD_TIME	Config	R/W	0000 1100	IPD_TIME[7:0]							
0x28	OFF_TIME	Config	R/W	0000 0001	OFF_TIME[7:0]							
0x29	DUTY_MIN	Config	R/W	0001 1001	DUTY_MIN[-1:-8]							
0x2A	OC_TIME	Config	R/W	0100 0000	OC_TIME[7:0]							
0x2B	VQM_START	Config	R/W	1111 1111	VQM_START[-1:-8]							
0x2C	VQM_RAMP	Config	R/W	0001 0000	VQM_RAMP[-1:-8]							
0x2D	VQM_TIME	Config	R/W	0001 0000	VQM_TIME[7:0]							
0x2E	HALL_RANGE	Config	R/W	0100 0000	HALL_RANGE[7:0]							
0x2F	VERSION	Data	R	0000 0001	VERSION[7:0]							
0x30	MTPA0_IQ	Config	R/W	0000 0000	MTPA0_IQ[-1:-8]							
0x31	MTPA0_ID	Config	R/W	0000 0000	Sign	MTPA0_ID[-1:-7]						
0x32	MTPA1_IQ	Config	R/W	0000 0000	MTPA1_IQ[-1:-8]							
0x33	MTPA1_ID	Config	R/W	0000 0000	Sign	MTPA1_ID[-1:-7]						
0x34	MTPA2_IQ	Config	R/W	0000 0000	MTPA2_IQ[-1:-8]							
0x35	MTPA2_ID	Config	R/W	0000 0000	Sign	MTPA2_ID[-1:-7]						
0x36	MTPA3_IQ	Config	R/W	0000 0000	MTPA3_IQ[-1:-8]							
0x37	MTPA3_ID	Config	R/W	0000 0000	Sign	MTPA3_ID[-1:-7]						
0x38	MTPA4_IQ	Config	R/W	0000 0000	MTPA4_IQ[-1:-8]							
0x39	MTPA4_ID	Config	R/W	0000 0000	Sign	MTPA4_ID[-1:-7]						
0x3A	MTPA5_IQ	Config	R/W	0000 0000	MTPA5_IQ[-1:-8]							
0x3B	MTPA5_ID	Config	R/W	0000 0000	Sign	MTPA5_ID[-1:-7]						
0x3C	MTPA6_IQ	Config	R/W	0000 0000	MTPA6_IQ[-1:-8]							
0x3D	MTPA6_ID	Config	R/W	0000 0000	Sign	MTPA6_ID[-1:-7]						
0x3E	MTPA7_IQ	Config	R/W	0000 0000	MTPA7_IQ[-1:-8]							
0x3F	MTPA7_ID	Config	R/W	0000 0000	Sign	MTPA7_ID[-1:-7]						
0x40	THETA	Config	R/W	0000 0000	THETA[14:7]							
0x41				0000 0000	THETA[6:-1]							
0x42	START_SPEED	Config	R/W	0000 0000	START_SPEED[15:8]							
0x43				0011 1100	START_SPEED[7:0]							
0x44	END_SPEED	Config	R/W	0000 0000	END_SPEED[15:8]							
0x45				0111 1000	END_SPEED[7:0]							
0x46	A1	Config	RW	0000 0000	Sign	A1[7:1]						
0x47				0000 0000	A1[0:-7]							

Hex Address	Name	Type	Access	Default Reset	B7	B6	B5	B4	B3	B2	B1	B0
0x48	A2	Config	R/W	0000 0000	Sign	A2[3:-3]						
0x49				0000 0000	A2[-4:-11]							
0x4A	START_VQ	Config	R/W	0001 0000	START_VQ[-1:-8]							
0x4B				0000 0000	START_VQ[-9:-16]							
0x4C	KINV	Config	R/W	0000 0000	0	KINV[13:7]						
0x4D				0001 0000	KINV[6:-1]							
0x4E				0110 0010	KINV[-2:-9]							
0x4F				0100 1101	KINV[-10:-17]							
0x50	VQ_MAX	Config	R/W	1101 0010	VQ_MAX[-1:-8]							
0x51				1001 1011	VQ_MAX[-9:-16]							
0x52	VQ_MIN	Config	RW	0000 0000	Sign	VQ_MIN[-1:-7]						
0x53				0000 0000	VQ_MIN[-8:-15]							
0x54	V_RATIO	Config	R/W	0001 1001	V_RATIO[9:2]							
0x55				0100 0000	V_RATIO[1:-6]							
0x56	TARGET_POWER	Config	R/W	0000 0000	TARGET_POWER[-2:-9]							
0x57				0000 0000	TARGET_POWER[-10:-17]							
0x58	SPEED_CONSTANT	Config	R/W	0000 1000	SPEED_CONSTANT[13:6]							
0x59				1000 1000	SPEED_CONSTANT[5:-2]							
0x5A	TARGET_SPEED	Config	R/W	0000 0100	TARGET_SPEED[15:8]							
0x5B				0000 0000	TARGET_SPEED[7:0]							
0x5C	R_FOC	Config	R/W	0000 0100	R_FOC[5:-2]							
0x5D				0000 0000	R_FOC[-3:-10]							
0x5E	L_FOC	Config	R/W	0000 0000	L_FOC[4:-3]							
0x5F				0000 0010	L_FOC[-4:-11]							
0x60			R/W	0001 1000	L_FOC[-12:-19]							
0x61	POLE_PAIR	Config	R/W	0000 0010	POLE_PAIR[7:0]							
0x62	FREQ	Config	R/W	0100 1100	FREQ[15:8]							
0x63				0100 1011	FREQ[7:0]							
0x64	F_A	Config	R/W	0000 0000	F_A[-1:-8]							
0x65				0100 0000	F_A[-9:-16]							
0x66	F_B	Config	R/W	0001 0000	F_B[-1:-8]							
0x67				0000 0000	F_B[-9:-16]							
0x68	F_C	Config	R/W	0000 1000	F_C[-1:-8]							
0x69				0000 0000	F_C[-9:-16]							
0x6A	DELTA_VQ	Config	R/W	0000 1000	DELTA_VQ[-1:-8]							
0x6B				0000 0000	DELTA_VQ[-9:-16]							
0x6C	TARGET_VQ	Config	R/W	0100 0000	TARGET_VQ[-1:-8]							
0x6D				0000 0000	TARGET_VQ[-9:-16]							
0x6E	FMAG_LOW	Config	R/W	0000 1000	FMAG_LOW[6:-1]							
0x6F				0000 0000	FMAG_LOW[-2:-9]							

Hex Address	Name	Type	Access	Default Reset	B7	B6	B5	B4	B3	B2	B1	B0
0x70	F_V	Config	R/W	0000 1000	F_V[-1:-8]							
0x71				0000 0000	F_V[-9:-16]							
0x72	VDC	Config	R/W	0000 0110	VDC[9:2]							
0x73				0000 0000	VDC[1:-6]							
0x74	RSENSE	Config	R/W	0000 0010	RSENSE[-1:-8]							
0x75				1000 1111	RSENSE[-9:-16]							
0x76	MAX_ERR	Config	R/W	0000 0000	MAX_ERR[7:0]							
0x77				0010 0000	MAX_ERR[-1:-8]							
0x78	R_STARTUP	Config	R/W	0000 0100	R_STARTUP[5:-2]							
0x79				0000 0000	R_STARTUP[-3:-10]							
0x7A	L_STARTUP	Config	R/W	0000 0000	L_STARTUP[4:-3]							
0x7B				0000 0010	L_STARTUP[-4:-11]							
0x7C				0001 1000	L_STARTUP[-12:-19]							
0x7D	MIN_DTHETA	Config	R/W	0101 0101	MIN_DTHETA[13:6]							
0x7E	TIME_ADJ	Config	RW	0010 0000	Sign	TIME_ADJ[1:-5]						
0x7F				0000 0000	TIME_ADJ[-6:-13]							
0x80	VQ	Data	R	0000 0000	Sign	VQ[-1:-7]						
0x81				0000 0000	VQ[-8:-15]							
0x82	VD	Data	R	0000 0000	Sign	VD[-1:-7]						
0x83				0000 0000	VD[-8:-15]							
0x84	VALPHA	Data	R	0000 0000	Sign	VALPHA[-1:-7]						
0x85				0000 0000	VALPHA[-8:-15]							
0x86	VBETA	Data	R	0000 0000	Sign	VBETA[-1:-7]						
0x87				0000 0000	VBETA[-8:-15]							
0x88	VU	Data	R	0000 0000	Sign	VU[-1:-7]						
0x89				0000 0000	VU[-8:-15]							
0x8A	VV	Data	R	0000 0000	Sign	VV[-1:-7]						
0x8B				0000 0000	VV[-8:-15]							
0x8C	VW	Data	R	0000 0000	Sign	VW[-1:-7]						
0x8D				0000 0000	VW[-8:-15]							
0x8E	TARGET_IQ2	Data	R	0000 0000	Sign	TARGET_IQ2[-1:-7]						
0x8F				0000 0000	TARGET_IQ2[-8:-15]							
0x90	TARGET_ID2	Data	R	0000 0000	Sign	TARGET_ID2[-1:-7]						
0x91				0000 0000	TARGET_ID2[-8:-15]							
0x92	MODE_B	Config	R/W	0000 0000	P_IPD	P_ISD				PROT_EN	PMODE[1:0]	
0x93	KU	Config	R/W	0000 0000	KU[7:0]							
0x94	KV	Config	R/W	0000 0000	KV[7:0]							
0x95	KW	Config	R/W	0000 0000	KW[7:0]							
0x96	R_VQ	Config	R/W	0000 0100	R_VQ[5:-2]							
0x97				0000 0000	R-VQ[-3:-10]							
0x98	FMAG	Data	R	0000 0000	FMAG[13:6]							

Hex Address	Name	Type	Access	Default Reset	B7	B6	B5	B4	B3	B2	B1	B0
0x99				0000 0000	FMAG[5:-2]							
0x9A	VBL_LMT	Config	R/W	0000 0000	VBL_LMT[-1:-8]							
0x9B	VBH_LMT	Config	R/W	1111 1111	VBH_LMT[-1:-8]							
0x9C	NTCH_LMT	Config	R/W	0000 0000	NTCH_LMT[-1:-8]							
0x9D	ITOTAL	Data	R	0000 0000	ITOTAL[2:-5]							
0x9E	IALPHA	Data	R	0000 0000	Sign	IALPHA[-1:-7]						
0x9F				0000 0000	IALPHA[-8:-15]							
0xA0	IBETA	Data	R	0000 0000	Sign	IBETA[-1:-7]						
0xA1				0000 0000	IBETA[-8:-15]							
0xA2	F_SPEED	Data	R	0000 0000	Sign	F_SPEED[15:9]						
0xA3				0000 0000	F_SPEED[8:1]							
0xA4	FTHETA_LPF	Data	R	0000 0000	FTHETA_LPF[14:7]							
0xA5				0000 0000	FTHETA_LPF[6:-1]							
0xA6	EALPHA	Data	R	0000 0000	Sign	EALPHA[-1:-7]						
0xA7				0000 0000	EALPHA[-8:-15]							
0xA8	EBETA	Data	R	0000 0000	Sign	EBETA[-1:-7]						
0xA9				0000 0000	EBETA[-8:-15]							
0xAA	VS2	Data	R	0000 0000	VS2[0:-7]							
0xAB				0000 0000	VS2[-8:-15]							
0xAC	IS2	Data	R	0000 0000	IS2[-1:-8]							
0xAD				0000 0000	IS2[-9:-16]							
0xAE	POWER_LPF	Data	R	0000 0000	Sign	POWER_LPF[-2:-8]						
0xAF				0000 0000	POWER_LPF[-9:-16]							
0xB0	ID	Data	R	0000 0000	Sign	ID[-1:-7]						
0xB1				0000 0000	ID[-8:-15]							
0xB2	IQ_LPF	Data	R	0000 0000	Sign	IQ_LPF[-1:-7]						
0xB3				0000 0000	IQ_LPF[-8:-15]							
0xB4	AD_DATA	Data	R	0000 0000	Sign	AD_DATA[10:4]						
0xB5				0000 0000	AD_DATA[3:0]				-	-	-	-
0xB6	VB	Data	R	0000 0000	VB[-1:-8]							
0xB7				0000 0000	VB[-9:-16]							
0xB8	KSCALE	Data	R	0000 0000	0	KSCALE[13:7]						
0xB9				0000 0010	KSCALE[6:-1]							
0xBA				0000 0000	KSCALE[-2:-9]							
0xBB				0000 0000	KSCALE[-10:-17]							
0xBC	ANGLE_ADJ	Data	R	0000 0000	Sign	ANGLE_ADJ[13:7]						
0xBD				0000 0000	ANGLE_ADJ[6:-1]							
0xC0	TARGET_IQ	Config	RW	0001 1000	Sign	TARGET_IQ[-1:-7]						
0xC1				0000 0000	TARGET_IQ[-8:-15]							
0xC2	KP_IQ	Config	R/W	0000 1000	KP_IQ[1:-6]							
0xC3				0000 0000	KP_IQ[-7:-14]							

Hex Address	Name	Type	Access	Default Reset	B7	B6	B5	B4	B3	B2	B1	B0
0xC4	KI_IQ	Config	R/W	0000 0000	KO_IQ[1:-6]							
0xC5				1000 0000	KI_IQ[-7:-14]							
0xC6	KE_IQ	Config	R/W	0100 0000	KE_IQ[1:-6]							
0xC7				0000 0000	KE_IQ[-7:-14]							
0xC8	VD_MAX	Config	R/W	1101 0010	VD_MAX[-1:-8]							
0xC9				1001 1011	VD_MAX[-9:-16]							
0xCA	VD_MIN	Config	RW	11111001	Sign	VD_MIN[-1:-7]						
0xCB				1001 1001	VD_MIN[-8:-15]							
0xCC	KP_ID	Config	R/W	0000 1000	KP_ID[1:-6]							
0xCD				0000 0000	KP_ID[-7:-14]							
0xCE	KI_ID	Config	R/W	0000 0000	KI_ID[1:-6]							
0xCF				1000 0000	KI_ID[-7:-14]							
0xD0	KE_ID	Config	R/W	0100 0000	KE_ID[1:-6]							
0xD1				0000 0000	KE_ID[-7:-14]							
0xD2	IQ_MAX	Config	R/W	1111 0011	IQ_MAX[-1:-8]							
0xD3				0011 0011	IQ_MAX[-9:-16]							
0xD4	IQ_MIN	Config	RW	0000 0000	Sign	IQ_MIN[-1:-7]						
0xD5				0000 0000	IQ_MIN[-8:-15]							
0xD6	KP_SP	Config	R/W	0000 0000	KP_SP[1:-6]							
0xD7				0100 0000	KP_SP[-7:-14]							
0xD8	KI_SP	Config	R/W	0000 0000	KI_SP[1:-6]							
0xD9				0001 0000	KI_SP[-7:-14]							
0xDA	KE_SP	Config	R/W	0100 0000	KE_SP[1:-6]							
0xDB				0000 0000	KE_SP[-7:-14]							
0xDC	TARGET_ID	Config	RW	0000 0000	Sign	TARGET_ID[-1:-7]						
0xDD				0000 0000	TARGET_ID[-8:-15]							
0xDE	IMAX	Config	R/W	1111 1111	IMAX[1:-6]							
0xDF				1110 0000	IMAX[-7:-14]							
0xE0	OFFSET1	Data	R	0000 0000	Sign	OFFSET1[-1:-7]						
0xE1				0000 0000	OFFSET1[-8:-15]							
0xE2	OFFSET2	Data	R	0000 0000	Sign	OFFSET2[-1:-7]						
0xE3				0000 0000	OFFSET2[-8:-15]							
0xE4	OFFSET3	Data	R	0000 0000	Sign	OFFSET3[-1:-7]						
0xE5				0000 0000	OFFSET3[-8:-15]							
0xE6	AD1	Data	R	0000 0000	Sign	AD1[10:4]						
0xE7				0000 0000	AD1[3:0]							
0xE8	AD2	Data	R	0000 0000	Sign	AD2[10:4]						
0xE9				0000 0000	AD2[3:0]							
0xEA	AD3	Data	R	0000 0000	Sign	AD3[10:4]						
0xEB				0000 0000	AD3[3:0]							

Hex Address	Name	Type	Access	Default Reset	B7	B6	B5	B4	B3	B2	B1	B0
0xEC	BS_STATUS11	Status	R	0000 0000	BS_STATUS11[7:0]							
0xED	BS_STATUS12	Status	R	0000 0000	BS_STATUS12[7:0]							
0xEE	BS_STATUS13	Status	R	0000 0000	BS_STATUS13[7:0]							
0xEF	BS_STATUS21	Status	R	0000 0000	BS_STATUS21[7:0]							
0xF0	BS_STATUS22	Status	R	0000 0000	BS_STATUS22[7:0]							
0xF1	BS_STATUS23	Status	R	0000 0000	BS_STATUS23[7:0]							
0xF2	F_DQ	Config	R/W	0000 1000	F_DQ[-1:-8]							
0xF3				0000 0000	F_DQ[-9:-16]							
0xF4	TARGET_IS2	Config	RW	0000 0000	TARGET_IS2[-1:-8]							
0xF5				0000 0000	TARGET_IS2[-9:-16]							
0XF6	ISD_SPEED	Data	R/W	0000 0000	ISD_SPEED[15:8]							
0xF7				1000 0000	ISD_SPEED[7:0]							
0xF8	HALL_OFFSET0	Data	R/W	0000 0000	HALL_OFFSET0[7:0]							
0xF9	HALL_OFFSET1	Data	R/W	0000 0000	HALL_OFFSET1[7:0]							

I²C Interface Protocol

I²C Timing

KTX9602 support I²C Standard mode as shown in Table 2 and Figure 5.

Table 2. Detail of I²C Timing Diagram

Symbol	Description	Standard Mode		Unit
		Min	Max	
F_{SCL}	SCL clock frequency	0	100	KHz
$t_{HD.STA}$	Hold time (repeated) start condition	4.0	-	μs
$t_{SU.STA}$	Setup time (repeated) start condition	4.7	-	μs
t_{LOW}	Low period of the SCL clock	4.7		μs
t_{HIGH}	HIGH period of the SCL clock	4.0		μs
$t_{HD.DAT}$	Data hold time; For I²C bus devices	0	3.45	μs
$t_{SU.DAT}$	Data setup time	250		ns
T_r	Rise time of SDA & SCL		1000	ns
T_f	fall time of SDA & SCL		300	ns
$t_{SU.STO}$	Setup time for stop condition	4.0		μs
t_{BUF}	Bus free time between stop & start	4.7		μs

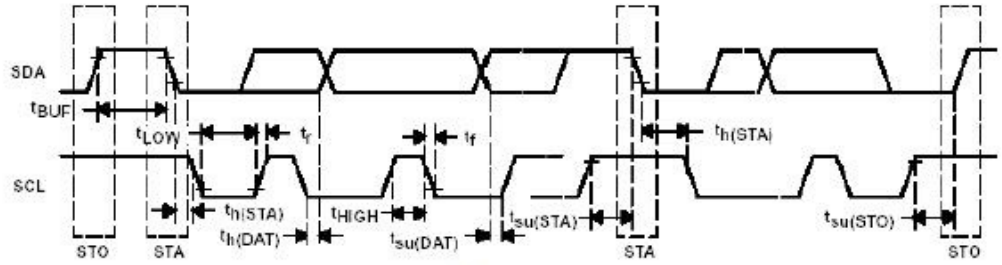


Figure 5. I²C Interface Timing

I²C Device Address

The KTX9602 is a slave I²C interface device that supports 7-bit slave addressing, with the read/write bit filling out the control byte. The slave address is fixed as <78H>. Figure 6 shows the detail of I²C addressing.

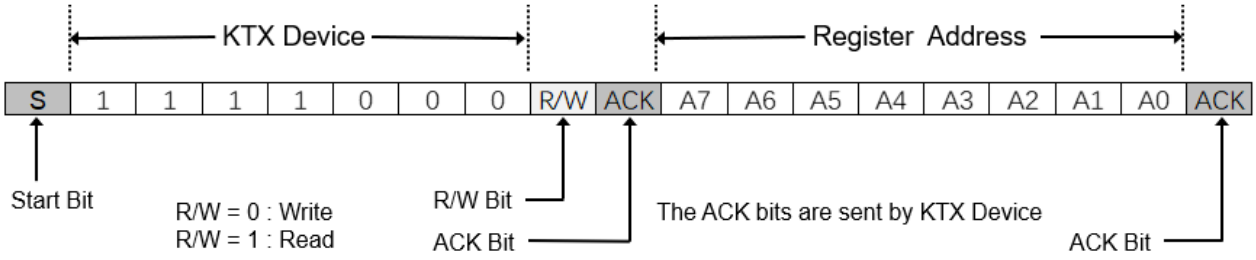


Figure 6. I²C Addressing

I²C Write Operation

The I²C write operation includes the control byte and register address sequence, as shown in the bottom of Figure 7. This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the KTX9602. The operation ends with a Stop (P) or Restart (SR) condition being generated by the master.

For every byte data transfer, if a Stop or Restart condition is generated during a data transfer, the data will not be written to the KTX9602. Some parameters are 16/24/32bits, please written to the KTX9602 by sequential mode, the data will not be written to the KTX9602 during byte mode transfer.

I²C Read Operation

I²C Read operations include the control byte sequence, as shown in the bottom of Figure 7.

This sequence is followed by another control byte (including the Start condition and ACK) with the R/W = 1.

KTX9602 then transmits the data contained in the addressed register. The sequence ends with the master generating a Stop or Restart condition.

I²C Sequential Write/Read

For transfer more than 1byte data please written to the KTX9602 by sequential mode.

For sequential operations (Write or Read), instead of transmitting a Stop or Restart condition after the data transfer, the master clocks the next byte pointed to by the address pointer. The sequence ends with the master sending a Stop or Restart condition. KTX9602 Address Pointer will roll over to address zero after reaching the last register address. Refer to Figure 7.

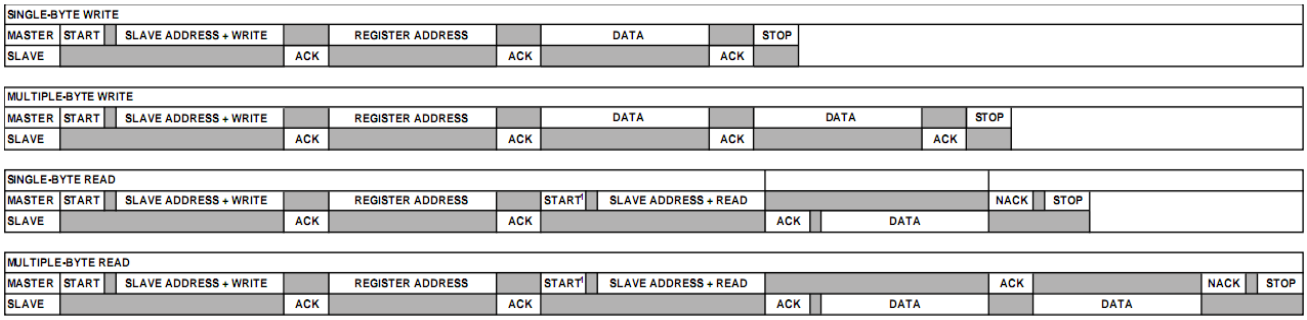
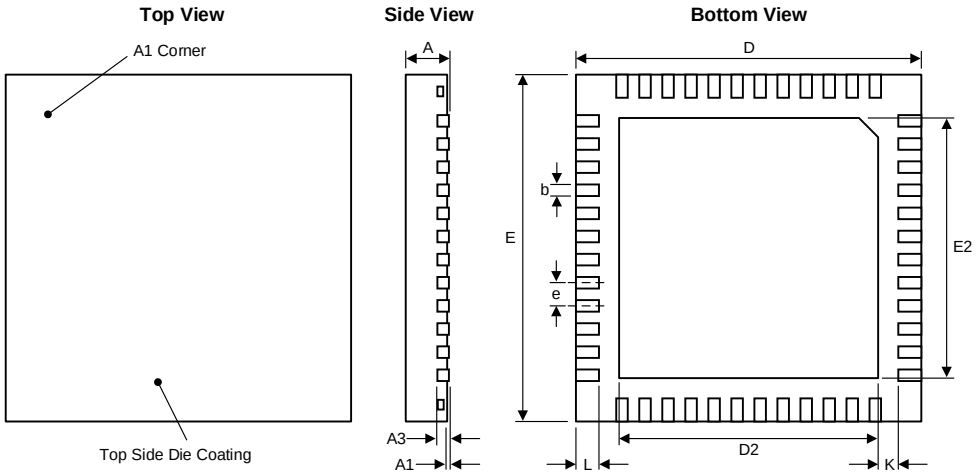


Figure 7. I²C Read/Write Operation

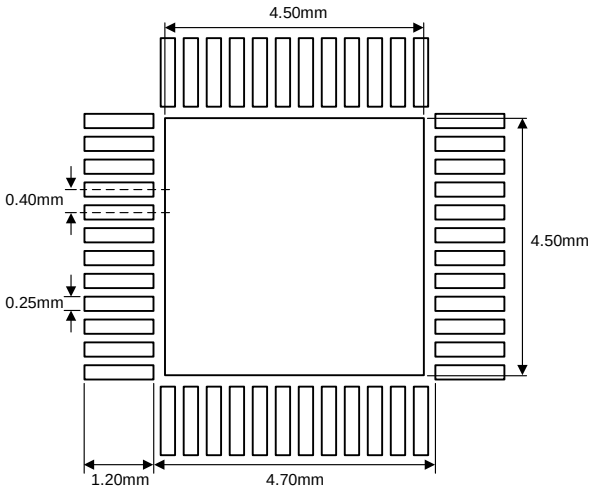
Packaging Information

WQFN66-48 (6.00mm x 6.00mm x 0.75mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.15	0.20	0.25
D	6.00 BSC		
D2	4.45	4.50	4.55
E	6.00 BSC		
E2	4.45	4.50	4.55
e	0.40 BSC		
K	0.20	–	–
L	0.35	0.40	0.45

Recommended Footprint



Kinetic Technologies cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Kinetic Technologies product. No intellectual property or circuit patent licenses are implied. Kinetic Technologies reserves the right to change the circuitry and specifications without notice at any time.