6A$_{RMS}$ VBUS I$_{SINK}$ Load Switch for 28V EPR Systems

Features

- 3V to 32V Operating Voltage Range
- 35VDC Abs. Max. Rating at IN and OUT
- 6A Continuous Current Rating
- 24mΩ typ. On-Resistance from IN to OUT
- Soft-Start (SS) Limits Inrush Current
- Over-Voltage Protection (OVP) at IN
  - ▸ 33V, 100ns Internally Fixed
  - ▸ 4V to 33V External Resistor Programmable
- "Ideal Diode" Reverse-Current Protection (RCP)
  - ▸ V_F = 20mV and 15µs Fast Recovery
- Short-Circuit Protection (SCP) during & after SS
- 12A, 150ns Over-Current Protection (OCP)
- Over-Temperature Protection (OTP)
- Transient Voltage Suppression (TVS) at IN
  - ▸ ±100V Surge Protection (IEC61000-4-5)
  - ▸ ±30kV ESD Contact Discharge (IEC61000-4-2)
  - ▸ ±30kV ESD Air Gap Discharge (IEC61000-4-2)
- $\overline{EN}$ (KTS1898A) or EN (KTS1898B) Enable Logic
- Hiccup Mode Auto-Retry after Faults
- $\overline{ACOK}$ Open-Drain Output Flag
- -40°C to 85°C Operating Temperature Range
- 25-bump WLCSP 2.56 x 2.56mm (0.5mm pitch)

Brief Description

The KTS1898 is a USB VBUS safety management load switch for up to 165W current-sink input for 28V EPR systems. The input operating range is 3V to 32V with input/output withstand up to 35VDC. Ultra-fast over-voltage protection (OVP) is internally set to 33V, but optionally adjusted via external resistors. Low on-resistance minimizes heat and voltage droop. Reverse-current protection (RCP) acts as a 20mV "ideal diode" with fast recovery.

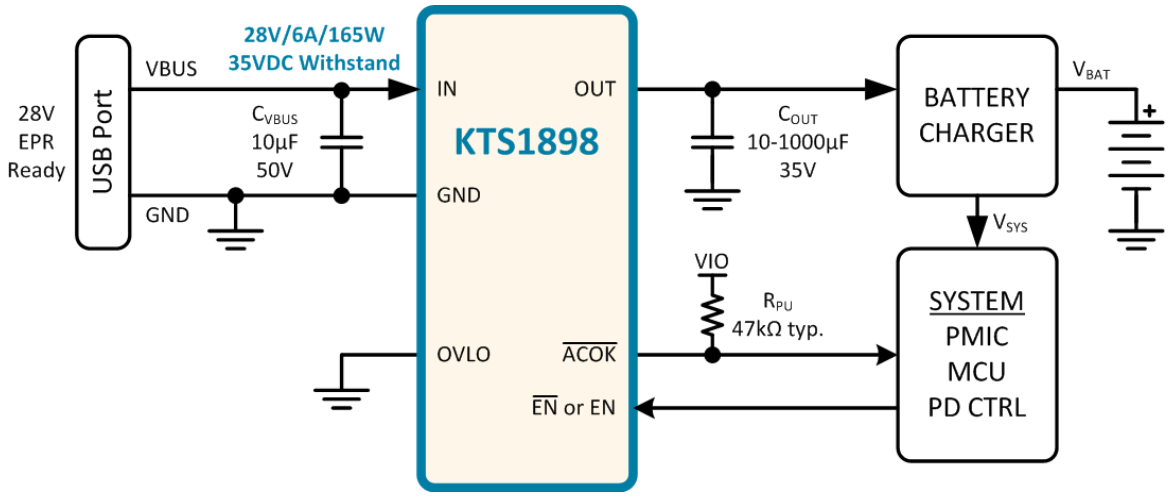
Additional safety management includes ultra-fast over-current protection (OCP), short-circuit protection (SCP) during and after soft-start, over-temperature protection (OTP), and an integrated transient voltage suppressor (TVS) for IEC industry standard ±30kV ESD and ±100V surge ratings.

The KTS1898 is packaged in advanced, fully "green" compliant, 2.56mm x 2.56mm, 25-bump Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Notebooks, Gaming PCs
- Mini Desktop PCs, Docking Stations, Monitors

Typical Application



Ordering Information

Part Number	Marking[1]	Enable Polarity	Operating Temperature	Package
KTS1898AEOAE-TA	SLXXYYZZZZ	$\overline{EN}$	-40°C to +85°C	WLCSP-25
KTS1898BEOAE-TA	RRXXYYZZZZ	EN	-40°C to +85°C	WLCSP-25

Pinout Diagram

WLCSP55-25

25-bump 2.560mm x 2.560mm x 0.555mm
WLCSP Package, 0.500mm pitch
Top Mark: WW = Device ID, XX = Date Code, YY = Assembly Code, ZZZZ = Serial Number

Pin Descriptions

Pin #	Name	Function
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5	OUT	Power Switch Output – connect to battery charger input (or V_{SYS} in systems without rechargeable batteries).
C1, C2, C3, C4, C5, D1, D2, D3, D4, D5	IN	Power Switch Input – connect to power input port (VBUS on USB port).
E3	$\overline{ACOK}$	Power Good Flag – active-low, open-drain logic output
E1	$\overline{EN}$	$\overline{Enable}$ – active-low logic input (KTS1898A)
	EN	Enable – active-high logic input (KTS1898B)
E2	OVLO	External OVLO Adjustment – connect to GND to use the internally fixed OVLO threshold. Connect an external resistive voltage divider from IN to OVLO to GND to adjust the OVLO threshold.
E4, E5	GND	Ground – high current ground return path during surge events

1. "SL" or "RR" is the Device ID, "XX" is the date code, "YY" is the assembly code, and "ZZZZ" is the serial number.

Absolute Maximum Ratings[3]

Symbol	Description	Value	Units
V_{IN}	IN to GND (continuous)	-0.3 to 35	V
	IN to GND (during IEC61000-4-5 surge event)	-5 to 48	
V_{OUT}	OUT to GND	-0.3 to 35	V
V_{IN-OUT}	IN to OUT	-34 to 35	V
V_{EN}, $V_{\overline{EN}}$	EN, $\overline{EN}$ to GND	-0.3 to 35	V
V_{OVLO}	OVLO to GND	-0.3 to V_{IN}	V
$V_{\overline{ACOK}}$	$\overline{ACOK}$ to GND	-0.3 to 6	V
I_{SW}	Maximum Switch Current (continuous)	6	A
	Peak Switch Current (5ms, OCP and Pd limited)	12	
T_J	Die Junction Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[4]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV
V_{ESD_CD}	IEC61000-4-2 Contact Discharge (IN)	±30	kV
V_{ESD_AGD}	IEC61000-4-2 Air Gap Discharge (IN)	±30	kV
V_{SURGE}	IEC61000-4-5 Surge (V_{IN} = 5V_{DC}+Surge, C_{IN} = 10µF, R_{LOAD} = 100Ω)	±100	V
	IEC61000-4-5 Surge (V_{IN} = 28V_{DC}+Surge, C_{IN} = 10µF, R_{LOAD} = 400Ω)	±100	V

Thermal Capabilities[5]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	55	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$ (T_J = 125°C)	1.82	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-18.2	mW/°C

3. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

4. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.

5. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions[6]

Symbol	Description	Value	Units
V_{IN}	Supply Voltage	3 to 32	V
V_{OUT}	Output Voltage	3 to 32	V
$V_{\overline{ACOK}}$	Power Good Flag Output Voltage[7]	0 to 5.5	V
V_{OVLO}	OVLO Adjust Input Bias Voltage	0 to 5.5	V
V_{EN}	Enable Logic Input Voltage	0 to 32	V
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Junction Operating Temperature Range	-40 to 125	°C
C_{IN}	Input Capacitance	1 to 10	µF
		50	V
C_{OUT}	Output Capacitance	10 to 1000	µF
		35 or 50	V

Electrical Characteristics[8]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C and V_{IN} = 3V to 32V. Typical values are specified at T_A = +25°C with V_{IN} = 5V.

Supply Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Operating Range		3		32	V
V_{UVLO}	Under-Voltage Lockout	V_{IN} rising threshold		2.7	2.9	V
		Hysteresis		160		mV
I_Q	No-Load Supply Current	Enabled, V_{IN} = 5V, OUT = open		218		µA
		Enabled, V_{IN} = 20V, OUT = open		267		
		Enabled, V_{IN} = 28V, OUT = open		292		
I_{SHDN}	Shutdown Supply Current	Shutdown, V_{IN} = 5V, OUT = open		1.1		µA
		Shutdown, V_{IN} = 20V, OUT = open		3.0		
		Shutdown, V_{IN} = 28V, OUT = open		3.8		
V_{OUT}	Output Voltage Operating Range		3		32	V
I_{OUT_RCP}	Output Supply Current in RCP	Enabled, V_{IN} = 0V, V_{OUT} = 5V		220		µA

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6. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

7. $\overline{ACOK}$ is an open-drain output flag. Use external pull-up resistor to a suitable I/O voltage. If unused, leave floating or connect to ground.

8. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

Electrical Characteristics (continued)[9]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C and V_{IN} = 3V to 32V. Typical values are specified at T_A = +25°C with V_{IN} = 5V.

TVS Surge Clamp Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{TVS_WRK}	Clamp Working Voltage	Positive Working Voltage			35	V
		Negative Working Voltage	0			
V_{TVS_CLMP}	Clamp Breakdown Voltage	I_{IN} = 10mA	38	41	44	V
		I_{IN} = -10mA	-1	-0.6		
V_{TVS_SRG}	Clamp Surge Voltage[10]	+100V surge		44		V
		-100V surge		-2		

Logic Pin Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High (EN, $\overline{EN}$)		1.2			V
V_{IL}	Input Logic Low (EN, $\overline{EN}$)				0.4	V
R_{I_PD}	Input Logic Pull-Down ($\overline{EN}$)			1		MΩ
I_{I_LK}	Input Logic Leakage (EN)	V_I = 5V V_I = 20V	-1 -1		1 1	µA µA
V_{OL}	Output Logic Low ($\overline{ACOK}$)	I_{O_SINK} = 1mA		0.01	0.2	V
I_{O_LK}	Output Logic High-Z Leakage ($\overline{ACOK}$)	V_O = 5V	-1		1	µA

Switch Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON}	Switch On-Resistance[11]	V_{IN} = 5V		24	30	mΩ
		V_{IN} = 20V[10]		24	30	
		V_{IN} = 28V[10]		24	30	
I_{IN_OFF}	Switch Off-Leakage at IN	Shutdown, V_{IN} = 5V, V_{OUT} = 0V		1.1		µA
		Shutdown, V_{IN} = 20V, V_{OUT} = 0V		3.0		
		Shutdown, V_{IN} = 28V, V_{OUT} = 0V		3.8		
I_{OUT_OFF}	Switch Off-Leakage at OUT	Shutdown, V_{IN} = 0V, V_{OUT} = 5V		1.0		µA
		Shutdown, V_{IN} = 0V, V_{OUT} = 20V		1.4		
		Shutdown, V_{IN} = 0V, V_{OUT} = 28V		2.3		

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9. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.
10. Guaranteed by design, characterization and statistical process control methods; not production tested.
11. Tested in test mode with RCP disabled, using ≤ 240mA output current, at room temperature.

Electrical Characteristics (continued)[12]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C and V_{IN} = 3V to 32V. Typical values are specified at T_A = +25°C with V_{IN} = 5V.

Soft-Start (SS) Specifications (see Figure 1)

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{HICCUP}	Hiccup Retry Time after fault[13, 14]	After OCP/OVP/OTP is triggered		72		ms
t_{DEB}	Soft-Start Debounce Time[15]	V_{IN} = 5V	10	19	25	ms
t_R	Soft-Start V_{OUT} Rising Slew-Rate Ramp Time[16]	V_{IN} = 5V	1	3.5	5	ms
		V_{IN} = 28V	1	3.0	5	
I_{LIM_SS}	Soft-Start Current Limit	V_{IN} = 5V to 28V		2.7		A
t_{LIM_SS}	Soft-Start Current Limit Done Time[13]	V_{IN} = 5V to 28V		8		ms
$t_{\overline{ACOK}}$	Power Good Flag Delay after t_{LIM_SS}[13]	V_{IN} = 5V to 28V		4.5		ms
t_{DOFF}	Turn-Off Delay Time[13, 17]	V_{IN} = 5V to 28V	0	1	10	µs

Over-Voltage Protection (OVP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OVP}	Internally Fixed Over-Voltage Protection	V_{IN} rising OVP threshold	32	33	34	V
		Hysteresis, V_{OVLO} = 0V		200		mV
t_{OVP}	OVP Response Time[13, 18]	R_L = 100Ω, C_{OUT} = 0µF, V_{IN} > V_{OVP}, V_{OVLO} = 0V		100		ns
t_{OVP_REC}	OVP Recovery Time[13, 19]		t_{HICCUP}+t_{DEB}+t_R			ms
V_{OVLO}	Externally Adjustable Over-Voltage Lockout	V_{OVLO} enable threshold	0.12	0.175	0.23	V
		V_{OVLO} rising OVP threshold	1.19	1.24	1.29	V
		Hysteresis		25		mV
t_{OVLO}	OVLO Response Time[13, 20]	R_L = 100Ω, C_{OUT} = 0µF		300		ns
t_{OVLO_REC}	OVLO Recovery Time[13]		t_{HICCUP}+t_{DEB}+t_R			ms

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12. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
13. Guaranteed by design, characterization and statistical process control methods; not production tested.
14. t_{HICCUP} is time from protection triggers until the start of Soft-Start Debounce Time.
15. t_{DEB} is time from enabled logic and V_{UVLO} < V_{IN} < V_{OVP} until V_{OUT} = 10%*V_{IN}.
16. t_R is time from V_{OUT} = 10%*V_{IN} until V_{OUT} = 90%*V_{IN}.
17. t_{DOFF} is time from enable logic until V_{OUT} begins to fall.
18. t_{OVP} is time from V_{IN} > V_{OVP} until V_{OUT} stops rising.
19. t_{OVP_REC} is time from V_{IN} < V_{OVP} until V_{OUT} = 90%*V_{IN}.
20. t_{OVLO} is time from V_{OVLO} rises above its OVP threshold until V_{OUT} stops rising.

Electrical Characteristics (continued)[21]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_A = -40°C to +85°C and V_{IN} = 3V to 32V. Typical values are specified at T_A = +25°C with V_{IN} = 5V.

Reverse-Current Protection (RCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RCP}	RCP Droop Regulation Voltage	$V_{RCP} = V_{IN} – V_{OUT}$, I_{OUT} = 100mA	10	20	30	mV
t_{RCP_REC}	RCP Fast Recovery Time[22, 23]			15		µs

Over-Current Protection (OCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{OCP}	Over-Current Protection (OCP) Threshold[23]			12		A
t_{OCP}	OCP Response Time[23, 24]			150		ns
t_{OCP_REC}	OCP Recovery Time[23]		$t_{HICCUP}+t_{DEB}+t_R$			ms

Over-Temperature Protection (OTP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{OTP}	IC Junction Over-Temperature Protection[23]	T_J rising threshold		150		°C
		Hysteresis		20		°C
t_{OTP_REC}	OTP Recovery Time[23]		$t_{HICCUP}+t_{DEB}+t_R$			ms

21. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

22. t_{RCP_REC} is time from $V_{IN} = V_{OUT} - V_{RCP}$ until switch turns back on. Before measuring, first raise $V_{OUT} >> V_{IN}$ + 270mV.

23. Guaranteed by design, characterization and statistical process control methods; not production tested.

24. t_{OCP} is time from I_{OUT} >> 12A until switch turns off.

Timing Diagrams

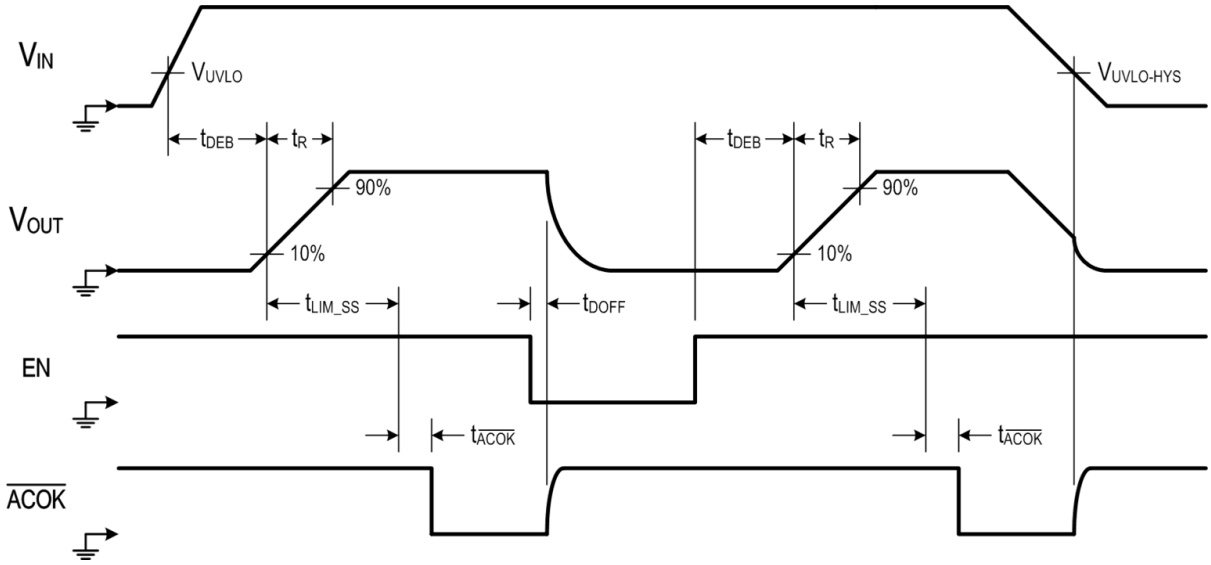


Figure 1. UVLO, Soft-Start and Turn-Off Timing Diagram

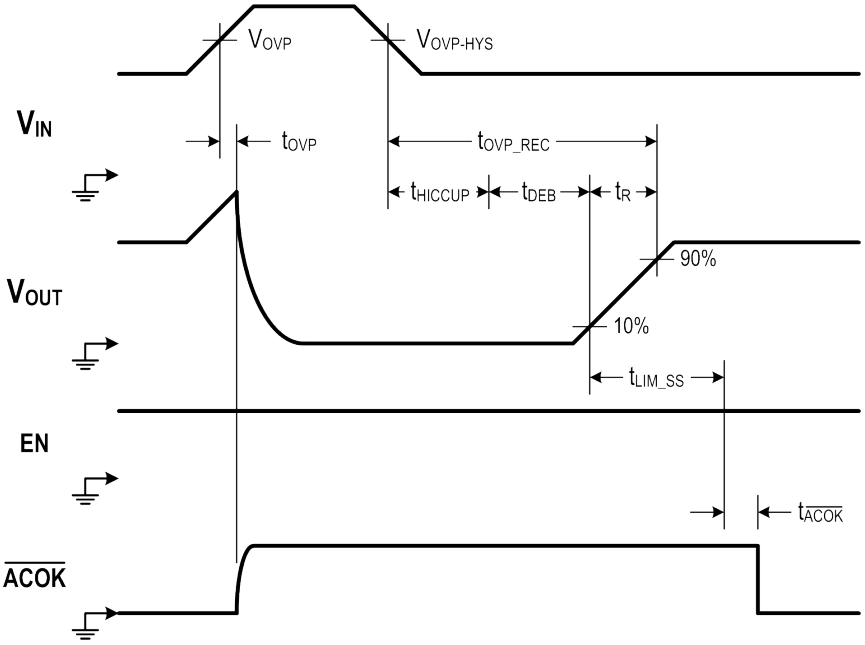


Figure 2. OVP Timing Diagram

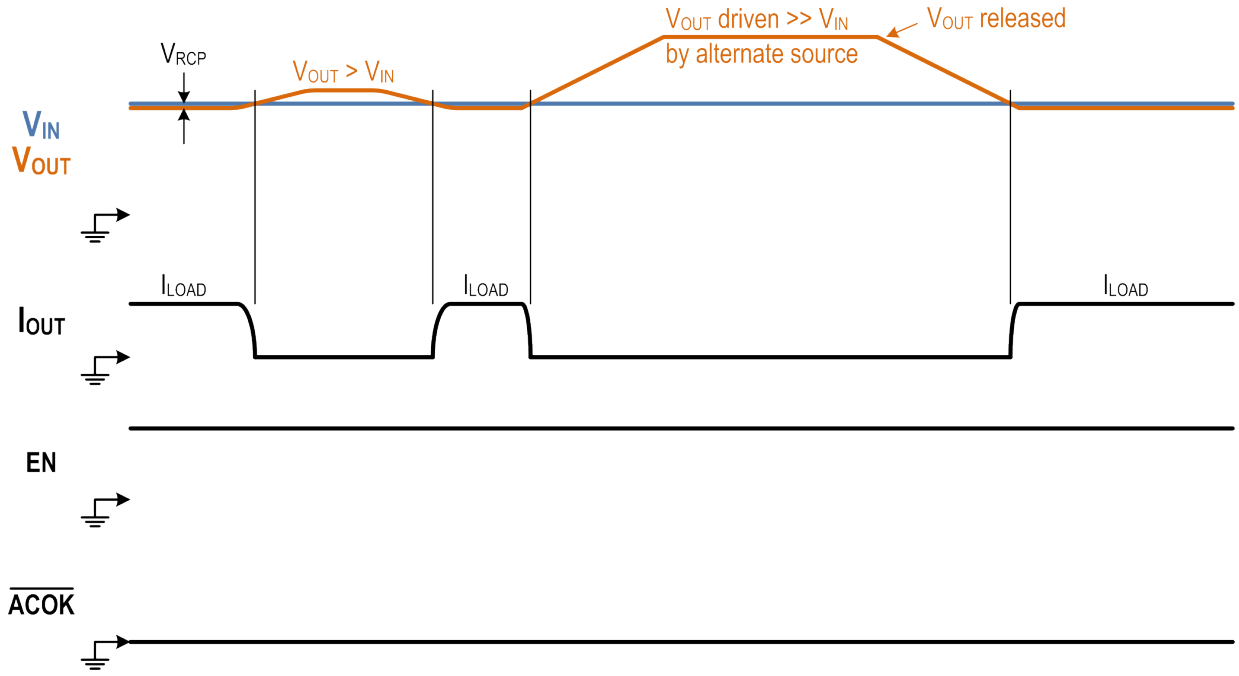


Figure 3. "Ideal Diode" RCP Timing Diagram

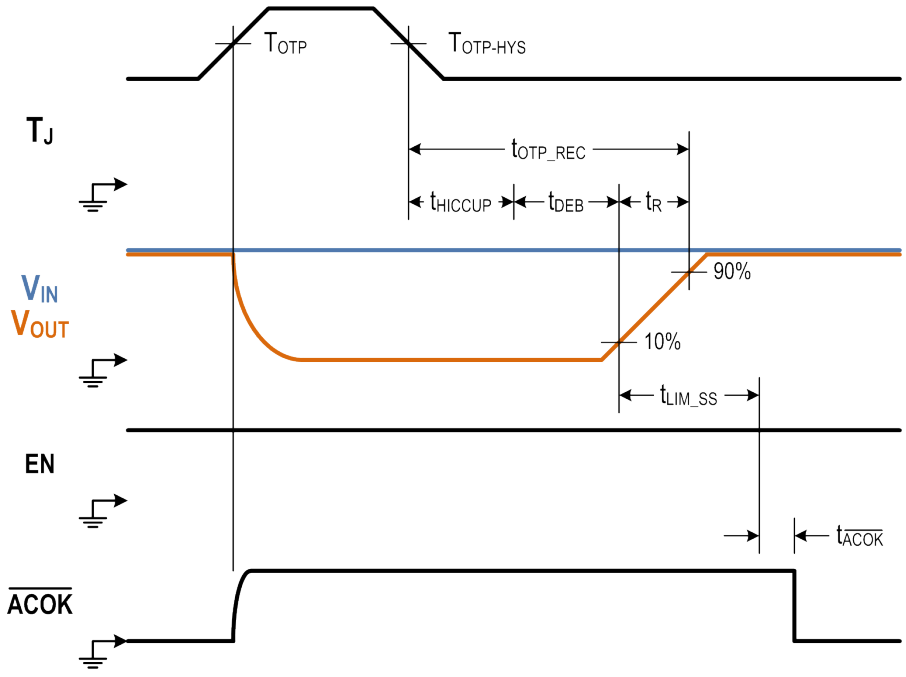


Figure 4. OTP Timing Diagram

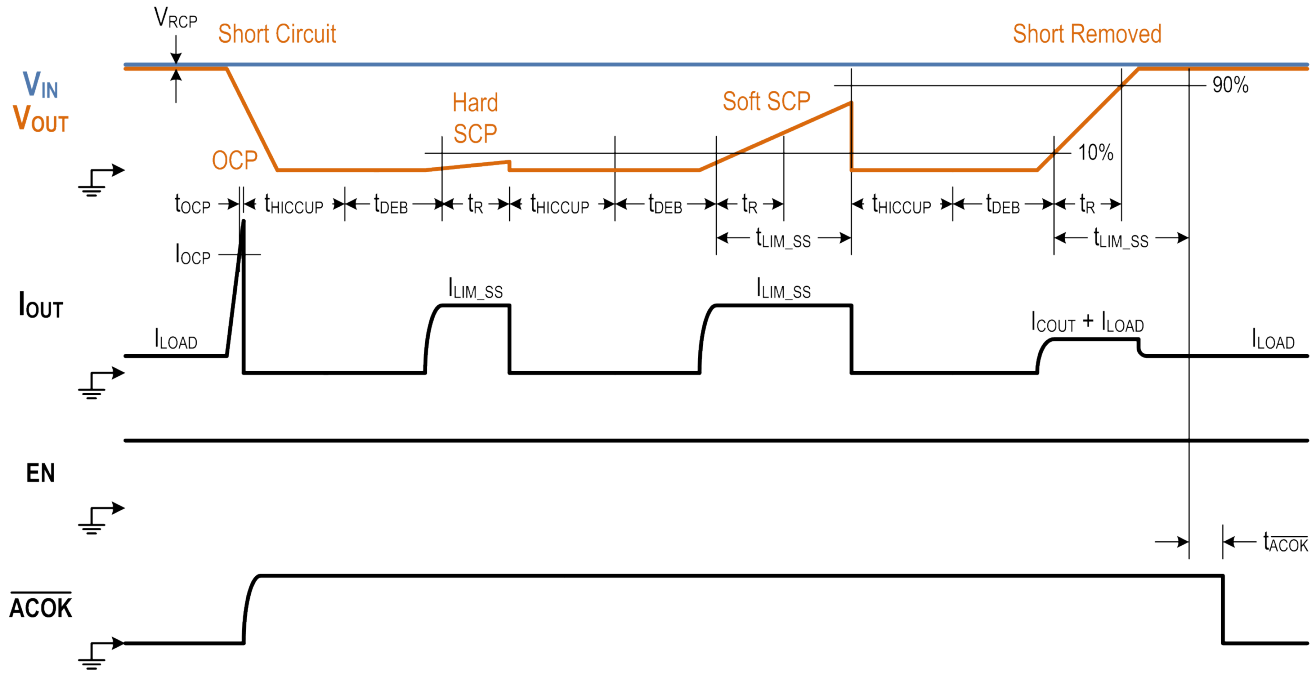
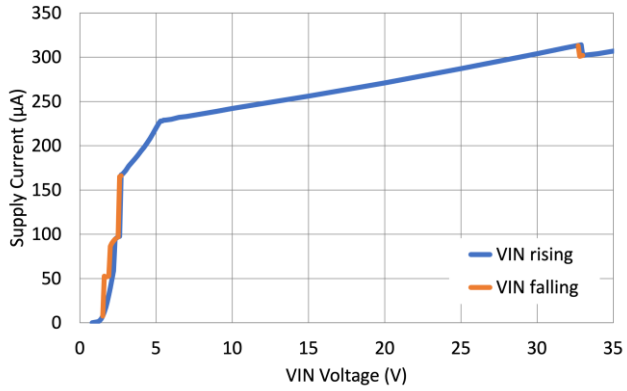


Figure 5. OCP and SCP Timing Diagram

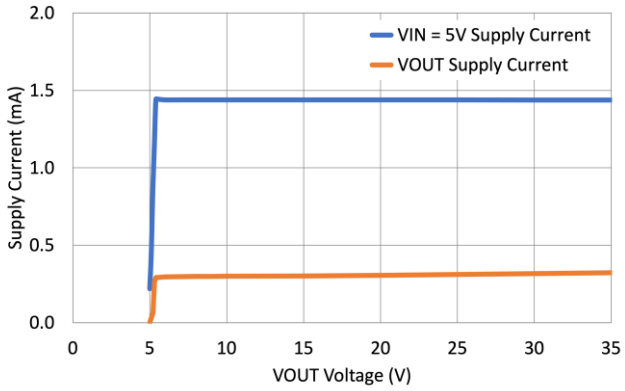
Typical Characteristics

C_{IN} = 10µF, C_{OUT} = 20µF, and T_A = +25°C unless otherwise noted.

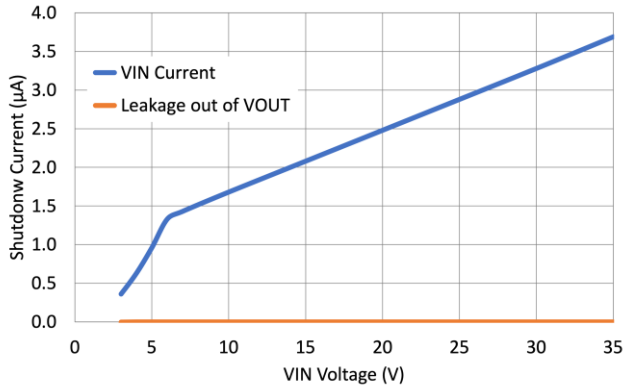
Supply Current vs. VIN
(enabled, no load)



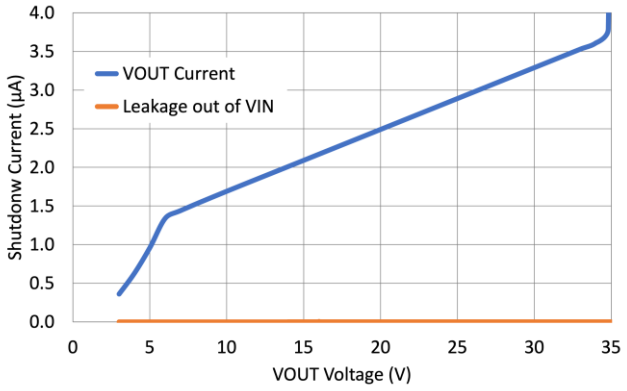
RCP Supply Current vs. VOUT
(VIN = 5V, enabled, no load)



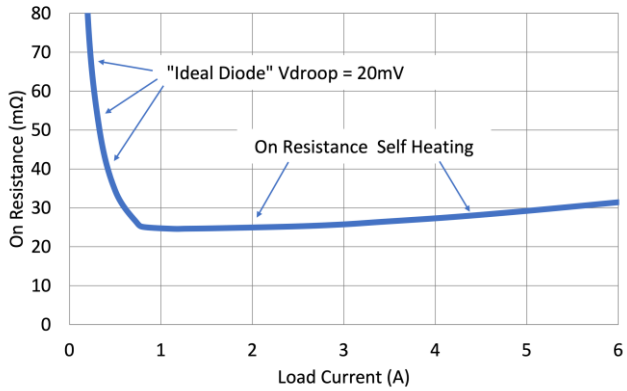
Shutdown Current & Leakage vs. VIN
(VOUT = 0V, disabled, no ambient light)



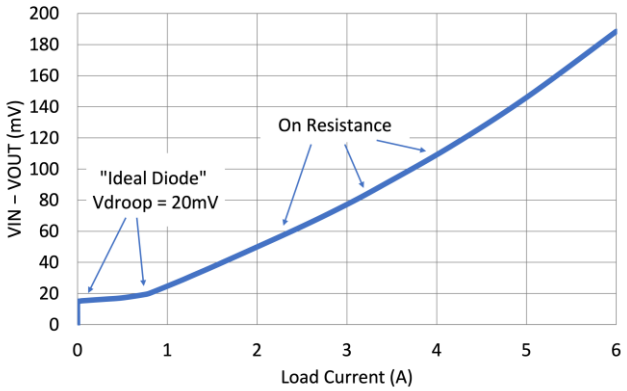
RCP Shutdown Current & Leakage vs. VOUT
(VIN = 0V, disabled, no ambient light)



On Resistance vs. Load Current
(VIN = 5 to 28V, enabled)



"Ideal Diode" Vdroop vs. Load Current
(VIN = 5 to 28V, enabled)



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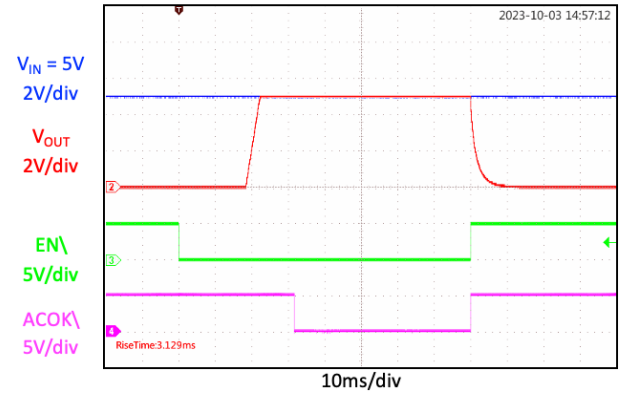
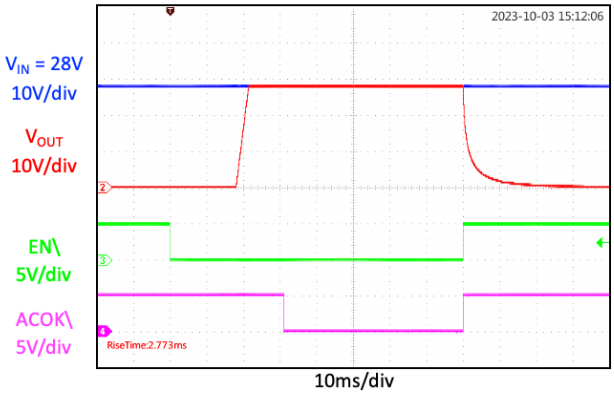
Typical Characteristics (continued)

C_{IN} = 10µF, C_{OUT} = 20µF, and T_A = +25°C unless otherwise noted.

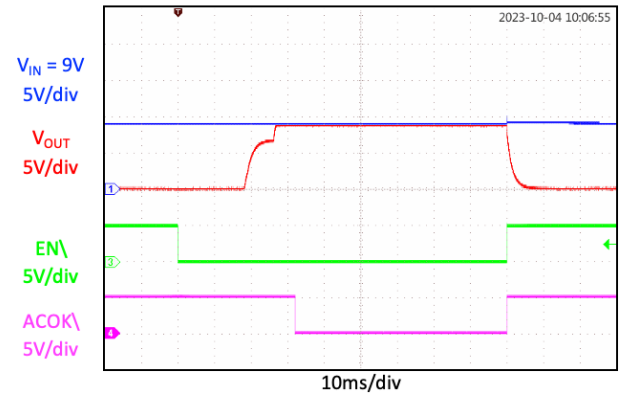
Enable, Soft-Start, Shutdown Response
(VIN = 5V, RLOAD = 100Ω)



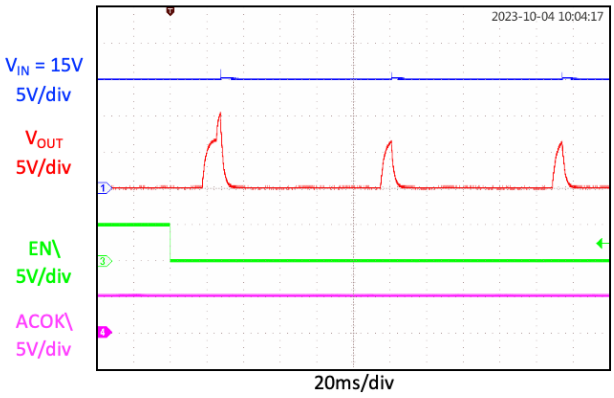
Enable, Soft-Start, Shutdown Response
(VIN = 28V, RLOAD = 400Ω)



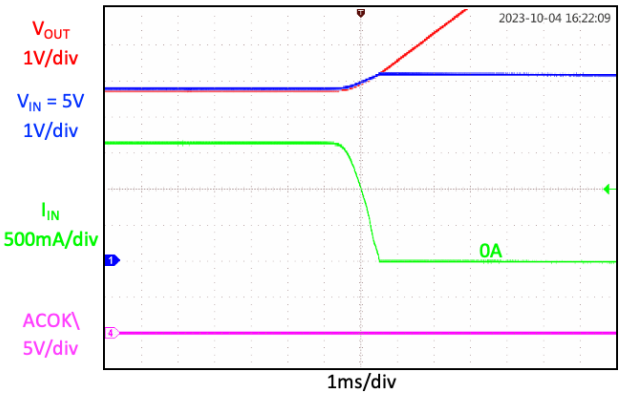
Heavy Load Soft-Start Response
(VIN = 9V, COUT = 1000µF, RLOAD = 2.5Ω)



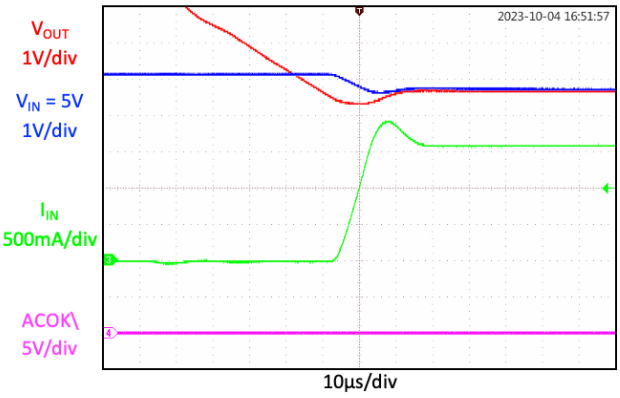
Over-Load Soft-Start & Auto-Retry Response
(VIN = 15V, COUT = 1000µF, RLOAD = 2.5Ω)



RCP Response
(VOUT = 5V → 9V, RCABLE = 200mΩ, RLOAD = 3Ω)



RCP Fast Recovery
(VOUT = 9V → 5V, RCABLE = 200mΩ, RLOAD = 3Ω)



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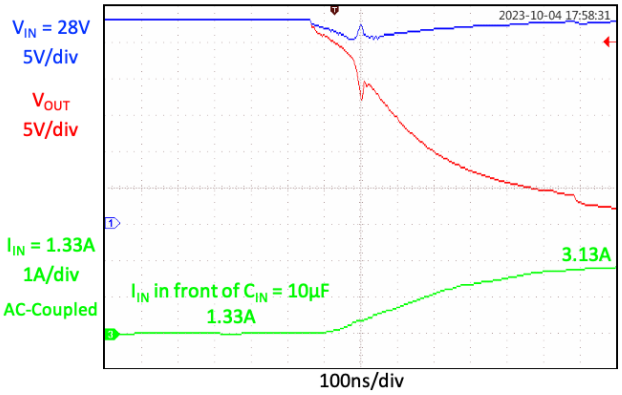
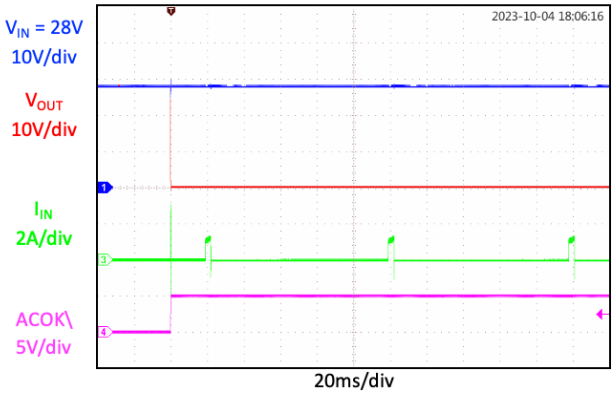
Typical Characteristics (continued)

C_{IN} = 10µF, C_{OUT} = 20µF, and T_A = +25°C unless otherwise noted.

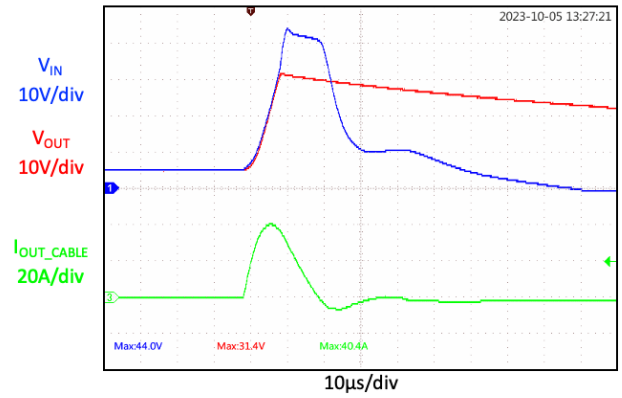
OCP/SCP Response
(VOUT = 28V → Short Circuit, RLOAD = 21Ω)



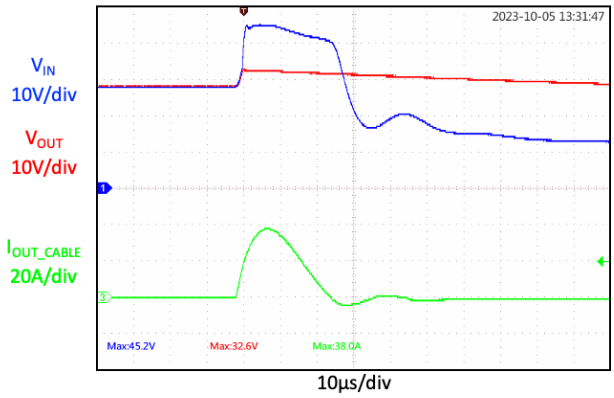
SCP Response with Auto-Retry
(VOUT = 28V → Short Circuit)



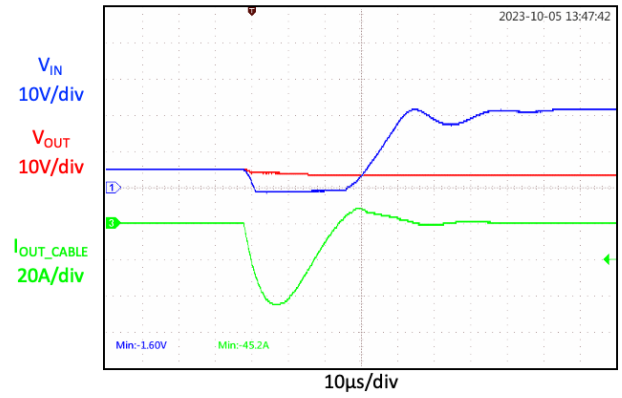
Surge Transient Response
(VIN = 5VDC + 100V Surge, enabled)



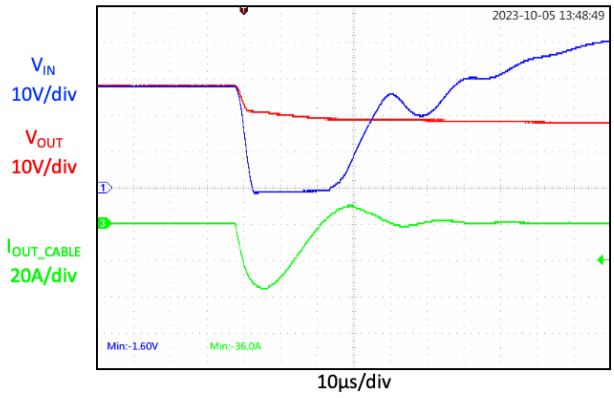
Surge Transient Response
(VIN = 28VDC + 100V Surge, enabled)



Surge Transient Response
(VIN = 5VDC - 100V Surge, enabled)



Surge Transient Response
(VIN = 28VDC - 100V Surge, enabled)



Functional Block Diagram

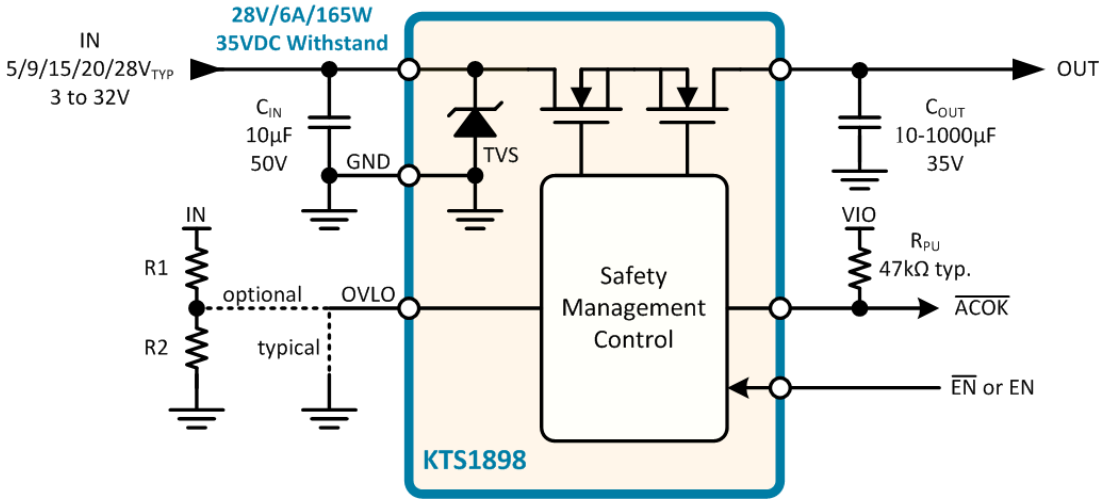


Figure 6. Functional Block Diagram

Functional Description

The KTS1898 is a slew-rate controlled, 24mΩ (typ) low resistance MOSFET switch intended to be inserted between a power source and a load to isolate and protect against abnormal voltage and current conditions. Featuring slew-rate controlled soft-start and soft-start current limit to prevent excessive large inrush current, the KTS1898 also features several additional protection functions. These include input over-voltage protection, "ideal diode" reverse-current protection with fast recovery, output short-circuit protection, over-current protection, over-temperature protection, and input transient voltage suppression for ±100V surge, ±30kV contact ESD, and ±30kV air-gap ESD protections.

Operating from a wide input voltage range of 3V to 32V, the KTS1898 is optimized for USB Type-C Power Delivery (PD) current-sink applications up to 28V extended power range (EPR) that require essential protection and enhanced system reliability. While in the OFF state, the KTS1898 blocks voltages of up to 35V on the IN and OUT pins and prevents current flow. While in the ON state, the KTS1898 withstands voltages of up to 35V on the IN and OUT pins, passes valid input voltages and current from IN to OUT, and blocks reverse current from OUT to IN. Due to the ideal-diode behavior, two or more KTS1898 parts can be used in parallel to support systems that may be charged or powered from multiple ports.

Shutdown and Enable

The KTS1898A has $\overline{EN}$ active-low input logic with internal 1MΩ pull-down resistor. The KTS1898B has EN active-high input logic. When disabled, the main power MOSFETs are turned off, and the device enters low-power shutdown mode. During shutdown mode, the output ESD/surge clamp continues to protect the IC and system. When enabled, all additional protection circuits are active, and if no fault condition exists, the main power MOSFETs are turned ON.

Under-Voltage Lockout (UVLO)

The UVLO function keeps the switches in the OFF state when the input voltage is below the UVLO threshold, regardless of the enable logic level. When the input voltage is above the UVLO threshold and the device is enabled via logic input and there are no fault conditions, the switches are enabled to the ON state.

Soft-Start (SS)

The internal soft-start function allows the KTS1898 to charge a total output capacitance of 1000µF to 5V without excessive in-rush current. Soft-start controls the output voltage slew-rate ramp time. Use the below formula to calculate the current required to charge C_{OUT}:

$$I_{IN\_SS} = I_{LOAD} + C_{OUT}\left(\frac{V_{IN}}{t_R}\right)$$

where t_R = 3.5ms. In either case, the soft-start time is somewhat fast to reduce power dissipation in the KTS1898 during soft-start.

Note that in addition to the soft-start voltage ramp, a simultaneous soft-start current limit of 2.7A prevents excessive heat when starting into an output short-circuit condition or a large total output capacitance. This current limit turns off after 8ms (lasting several milliseconds longer than the soft-start voltage ramp). After an additional 4.5ms delay, if V_{OUT} is near V_{IN}, the $\overline{ACOK}$ flag indicates a power good condition. See the *Heavy Load Soft-Start Response* in the *Typical Characteristics* section.

Over-Voltage Protection (OVP)

When EN = H or $\overline{EN}$ = L, the switch is logically enabled. However, if $V_{IN} > V_{OVP}$, the power switch is disabled due to an OVP fault. Once V_{IN} drops below V_{OVP}, no other fault is detected, and EN = H or $\overline{EN}$ = L, the power switch is automatically re-enabled after the hiccup time expires via the soft-start debounce and ramp times.

The OVLO pin is used to adjust the over-voltage threshold externally. The default internal over-voltage threshold is 33V when the OVLO pin is tied to GND. Biasing the OVLO pin with a resistive voltage divider adjusts the over-voltage threshold from 4V to 33V as in the below formula:

$$V_{OVP} = V_{OVLO}\left(1 + \frac{R1}{R2}\right)$$

where V_{OVLO} = 1.24V. Connect R1 from IN to OVLO. Connect R2 from OVLO to ground. See Figure 6.

Over-Current Protection (OCP)

The KTS1898 includes output over-current protection (OCP) at 12A that protects the IC from damage when an over-current or short-circuit event suddenly appears. The OCP circuit disables the power switch, so the current becomes zero. After an OCP event, if no other fault is detected, and EN = H or $\overline{EN}$ = L, the power switch is re-enabled after the hiccup time expires via the soft-start debounce and ramp times.

Short-Circuit Protection (SCP)

The KTS1898 includes output short-circuit protection (SCP). If an SCP event occurs while the KTS1898 is already enabled and working, OCP is the first line of defense and responds very quickly. In this case, the current from C_{IN} through the switch to C_{OUT} increases very rapidly. For SCP events that do not reach OCP, if V_{OUT} droops significantly below V_{IN}, it is also detected as a soft-short event. In case of auto-retry or simply starting into a pre-existing SCP condition, the KTS1898 furthermore includes SCP detection during soft-start if V_{OUT} is not ramping up. The KTS1898 remains undamaged during continuous SCP events. The hiccup time reduces the average power dissipation during extended SCP conditions.

"Ideal Diode" Reverse-Current Protection (RCP)

The KTS1898 offers reverse-current protection regardless of the enable logic level. When disabled, all current flow is blocked. When enabled, the RCP acts as a voltage droop regulator. Once the voltage on V_{OUT} is higher than V_{IN} minus 20mV, the RCP circuit reduces the MOSFET gate drive to try and maintain the regulated 20mV droop, thereby acting as an "ideal diode" with Vf = 20mV. See Figure 7. This control method blocks all reverse current within the RCP control loop bandwidth. The RCP circuit makes it possible to connect two or more USB

charging ports to a single charger input in a “diode-OR” configuration with autonomous reverse-current blocking.

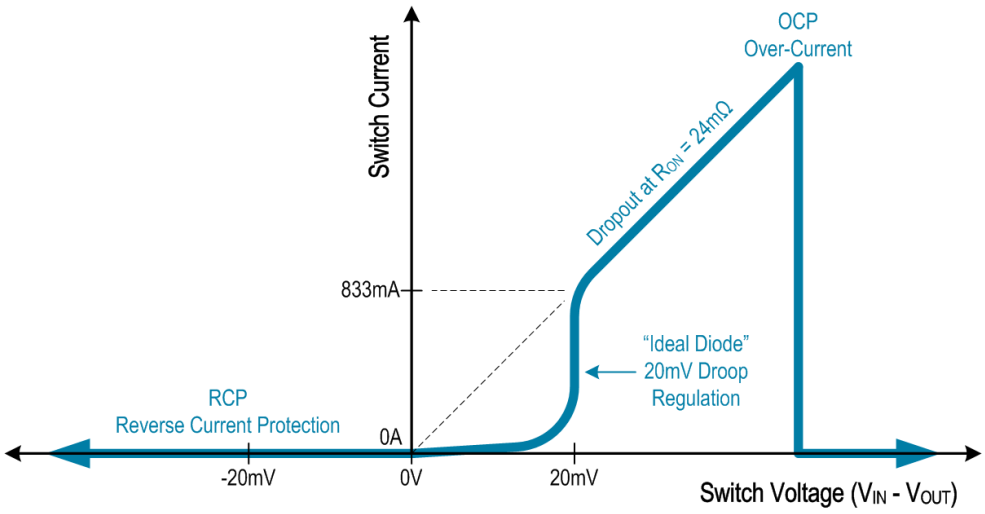


Figure 7. “Ideal Diode” Reverse-Current Protection V-I Curve

Over-Temperature Protection (OTP)

When device junction temperature exceeds 150°C, the OTP circuit disables the power switch. Once the device junction temperature decreases below 130°C, if no other fault is detected, and EN = H or $\overline{EN}$ = L, the power switch is re-enabled after the hiccup time expires via the soft-start debounce and ramp times.

Transient Voltage Suppression (TVS)

The KTS1898 integrates an active clamp transient voltage suppressor (TVS) from IN to GND. The TVS circuit provides protection to the KTS1898 and downstream circuits for IEC surge and ESD events. The protection is always active, whether the KTS1898 is enabled or disabled.

Auto-Retry

For all fault conditions that cause the switch to open, the KTS1898 will auto-retry via the soft-start debounce and ramp time. If any fault or the same fault is detected again, the switch will open again, and auto-retry will repeat. This continues until the fault is removed (normal operation) or EN = L or $\overline{EN}$ = H (shutdown) or V_{IN} is removed (UVLO). The hiccup timer extends the delay between auto-retry events, but only after the first retry.

$\overline{ACOK}$ Output Flag

The $\overline{ACOK}$ output is an open-drain output that requires an external pull-up resistor with recommended value in the 10kΩ to 200kΩ range. The $\overline{ACOK}$ pin indicates the fault status. When there is no fault (UVLO, OVP, OCP, SCP, and OTP are not triggered) and the power switch is ON, then the $\overline{ACOK}$ flag is pulled low to indicate the power is good. Otherwise, the $\overline{ACOK}$ flag is high impedance.

Applications Information

External Component Selection

Input Capacitor C_{IN}

For most applications, connect a 1µF to 10µF ceramic capacitor as close as possible to the device from IN to GND to minimize the effect of parasitic trace inductance. A 50V rated capacitor with X5R or better dielectric is recommended. For optimal surge and ESD performance, 10µF is preferred.

Output Capacitor C_{OUT}

For most applications, connect from 10µF to 1000µF total capacitance to the output. Typical applications use 30µF to 100µF as needed for system load-transients. At minimum, connect a 10µF ceramic capacitor as close as possible to the device from OUT to GND to minimize the effect of parasitic trace inductance. 35V or 50V rated capacitors with X5R or better dielectric are recommended. Lower voltage ratings may be acceptable when using the OVLO pin to set a lower over-voltage protection threshold.

Safe Operating Area (SOA)

See Figure 8 and Figure 9 for the SOA of the KTS1898. SOA curves are normally associated with discrete MOSFETs (which are sometimes co-package with a controller IC). In these competing systems, precautions are necessary to stay within the SOA area. However, the KTS1898 is a monolithic IC with all the integrated protection features to *automatically* keep its operation within the SOA area. For example, it includes over-voltage protection (OVP) and over-current protection (OCP) with very fast response times. It also includes over-temperature protection (OTP) that is measured on the same monolithic die as the integrated power MOSFETs. Additionally, soft-start is controlled with a voltage ramp and current limit protection (Soft-Start CLP) to safely soft-start even in systems with very high capacitance at the output. Furthermore, the integrated TVS and back-to-back MOSFET switch are optimized to work together as a system, including their tolerances over temperature and process corners.

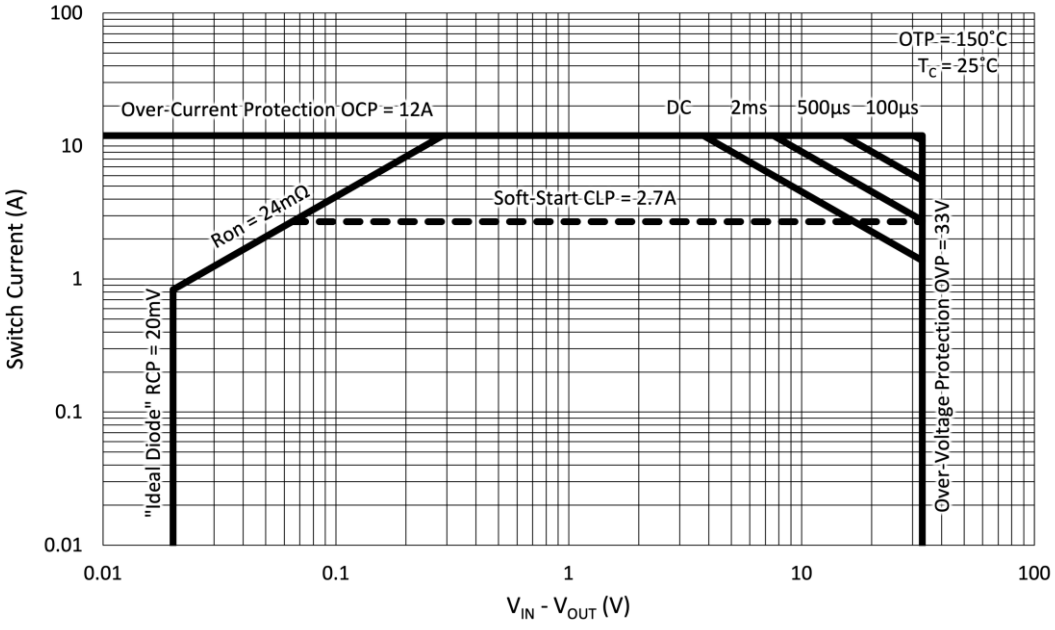


Figure 8. Safe Operating Area (SOA) for T_C = 25℃

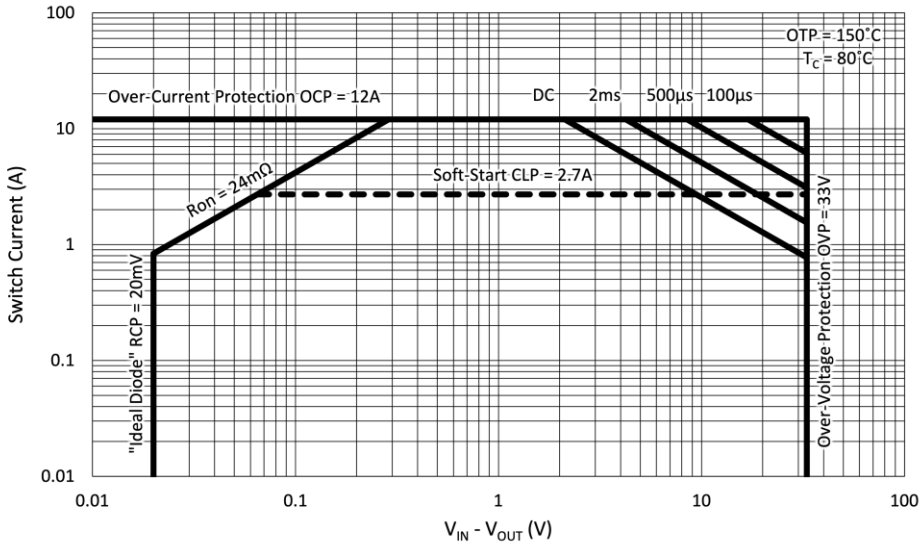


Figure 9. Safe Operating Area (SOA) for T_C = 80℃

Recommended PCB Layout

Good PCB thermal design is required to support heavy load currents. The KTS1898 EVB is designed with similar layout as Figure 10. Recommended PCB Layout, but it extends the fill area for the IN, OUT, and GND copper planes to about 4 square inches total area for increased thermal performance. Due to the number of bumps on IN and OUT, these two planes are especially important and should not be ignored. Adding back-side and/or buried-layer fill area with thermal vias also helps significantly.

Other than thermal concerns, the PCB layout for the KTS1898 is quite simple. Place the input and output capacitors near the IC. Connect the capacitor ground terminals together and to the GND pins using the top-side copper layer. Route the control signals on buried layers. For internally set 33V OVP, directly connect the OVLO pin to the GND pins (as shown in Figure 10).

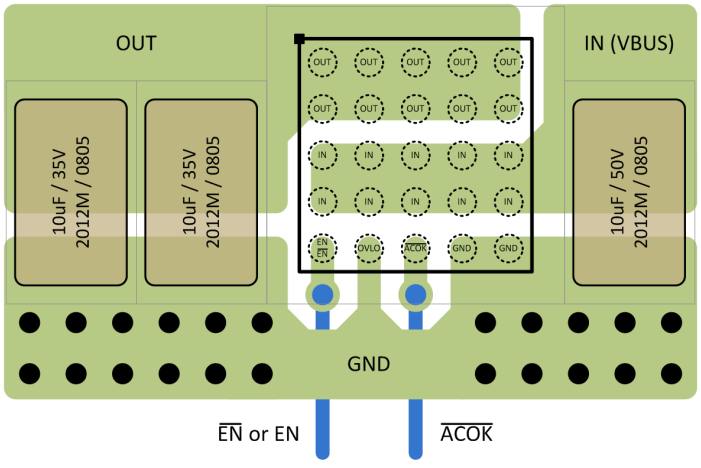
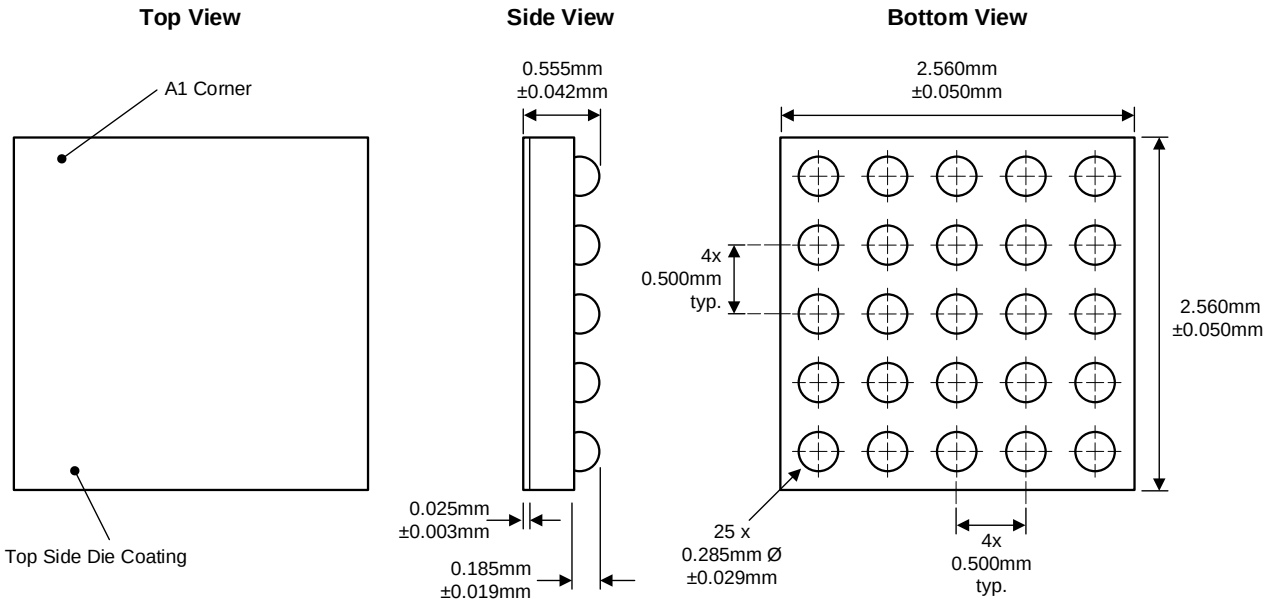


Figure 10. Recommended PCB Layout

Packaging Information

WLCSP55-25 (2.560mm x 2.560mm x 0.555mm)



Recommended Footprint