Surge Protected, Single Input, Dual Output Load Switch with OVP

Features

- Single Input, Dual Output Low-R_{ON} Switch
  - VBUS to VOUT: 20mΩ typ
  - VBUS to SYS: 35mΩ typ
  - Reverse Blocking on Both Switch Paths
- Wide Input Voltage Range: 2.7V – 13.2V
  - VBUS Abs Max: -6V to 28V
- Surge Protected VBUS
  - IEC61000-4-5: > ±200V
- ESD Protection
  - IEC61000-4-2 (Level 4) VBUS
    - Contact: ±8kV
    - Air Gap: ±15kV
  - HBM: 2kV All Pins
- Integrated Over-voltage Protection (OVP)
  - VBUS to VOUT: 13.9V
  - VBUS to SYS: 5.25V
- Maximum Continuous Current
  - VBUS to VOUT: 3.5A
  - VBUS to SYS: 6A
- OTG Compatible Power-Up
- Dual Enable Control with Independent Shutdown Control
  - Active LOW VBUS to VOUT
  - Active HIGH VBUS to SYS
  - Active HIGH Shutdown
- VBUS detection LDO
- VBUS to SYS FLAG
- VBUS Active Discharge Control Input
- Over Temperature Protection
- Pb-free 42-Bump, WLCSP 2.71mm x 3.01mm
- -40°C to 85°C Operating Temperature Range

Brief Description

The KTS1656 features two low resistance power switches configured as single input, dual output, change-over switch. The input to both switches is protected against VBUS surge voltages of up to ±200V, and is also protected against over-voltage, with preset trip points on both the VBUS-to-VOUT and VBUS-to-SYS paths, providing protection to downstream components from abnormal input conditions.

The main switch (VBUS-to-VOUT) is an active-LOW enabled, reverse-blocking 3.5A rated MOSFET, with an OVP trip point of 13.9V. The secondary switch (VBUS-to-SYS) is an active-HIGH enabled, reverse-blocking, 6.0A rated MOSFET, with an OVP trip point of 5.25V. The VBUS input is rated from -6V to 28V.

When VBUS is greater than 2.5V typ, the LDO output provides an "always ON" power source, regardless of the OVLO, $\overline{EN1}$ and EN2 state, to power downstream components, thereby permitting operation without an installed battery.

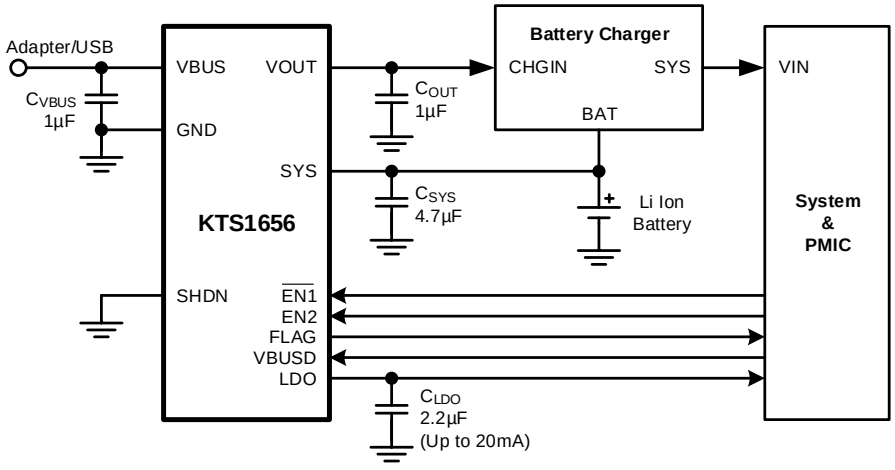
The KTS1656 also features an active-HIGH SHDN pin to conserve power and an over-temperature thermal protection.

The KTS1656 is packaged in advanced, fully "green" compliant, 2.71 x 3.01mm, Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Smartphones and Tablets
- Mobile Internet Devices
- Wearables and other Portable Devices

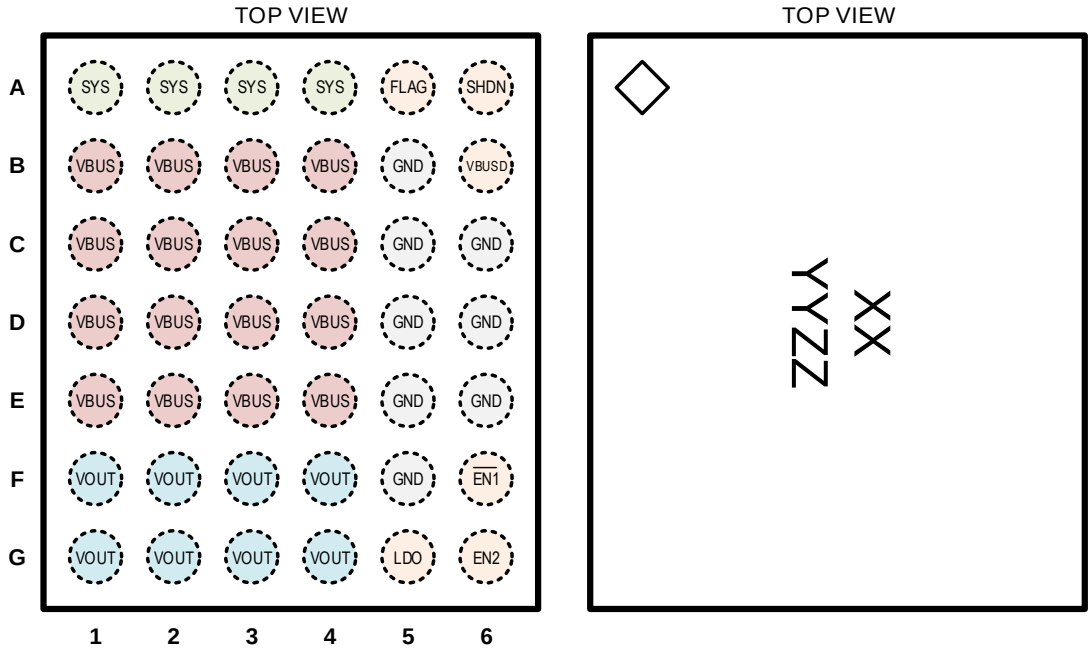
Typical Application



Pin Descriptions

Pin #	Name	Function
B1-B4, C1-C4, D1-D4, E1-E4	VBUS	Input to the power switches and device supply
F1-F4, G1-G4	VOUT	Power switch output to load
A1-A4	SYS	Power switch output to battery
G5	LDO	Regulated output whenever VBUS is present and SHDN is low
A5	FLAG	Active HIGH CMOS output whenever VBUS-to-SYS path is enabled and not in OVLO
G6	EN2	Active HIGH enable with internal 1MΩ pull-down, for VBUS to SYS path only
F6	$\overline{EN1}$	Active LOW enable with internal 1MΩ pull-down, for VBUS to VOUT path only
A6	SHDN	Active HIGH input with internal 1MΩ pull-down, for device shutdown
B6	VBUSD	Active HIGH analog input to gate of VBUS active discharge FET with internal 1MΩ pull-down
B5, C5, C6, D5, D6, E5, E6, F5	GND	Ground

WLCSP-42



42-Bump 2.71mm x 3.01mm x 0.62mm
WLCSP Package, 0.4mm pitch

Top Mark
WW = Device ID Code = LA
XX = Date Code, YY = Assembly Code
ZZZZ = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VBUS	VBUS to GND (continuous)	-6 to 28	V
	VBUS to VOUT (continuous)	-6 to 28	
	VBUS to SYS (continuous)	-11	
VOUT	VOUT to GND	-0.3 to VBUS+0.3	V
SYS	SYS to GND	-0.3 to 6	V
SHDN, $\overline{EN1}$, EN2, LDO, FLAG, VBUSD	SHDN, $\overline{EN1}$, EN2, LDO, FLAG, VBUSD to GND	-0.3 to 6	V
VBUS-VOUT Current	VBUS to VOUT Continuous Current	3.5	A
	VBUS to VOUT Peak Current (5ms)	7.0	A
VBUS-SYS Current	VBUS to SYS Continuous Current	6.0	A
	VBUS to SYS Peak Current (5ms)	12.0	A
T_J	Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[2]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV
V_{ESD_CD}	IEC61000-4-2 Contact Discharge (VBUS)	±8	kV
V_{ESD_AGD}	IEC61000-4-2 Air Gap Discharge (VBUS)	±15	kV
V_{SURGE}	IEC61000-4-5 Surge (VBUS to GND)	±200	V

Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	74	°C/W
P_D	Maximum Power Dissipation at 25°C	1.7	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	13.6	mW/°C

Ordering Information

Part Number	Marking[4]	Operating Temperature	Package
KTS1656EUY-TR	LAXXYYZZZZ	-40°C to +85°C	WLCSP42

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
4. “LAXXYYZZZZ” is the device ID code, date code, assembly code and serial number.

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, V_{BUS} = 2.7V to 13.2V. Typical values are specified at room temperature (25°C) with V_{BUS} = 5V, I_{VBUS} ≤ 2A, SHDN = $\overline{EN1}$ = EN2 = LOW, LDO = OPEN, C_{VBUS} = 0.1µF, C_{LDO} = 4.7µF and T_A = 25°C.

Input

Symbol	Description	Conditions	Min	Typ	Max	Units
I_Q	Input Quiescent Current	V_{BUS} = 5V, $\overline{EN1}$ = EN2 = LOW (VOUT path normal operation)		220	290	µA
		V_{BUS} = 4V, $\overline{EN1}$ = EN2 = HIGH (SYS path normal operation)		380	550	
		V_{BUS} = 5.5V, $\overline{EN1}$ = EN2 = HIGH, SYS = 0V (SYS path in OVLO)		240	320	
		V_{BUS} = 15V, $\overline{EN1}$ = EN2 = LOW, VOUT = 0V (VOUT path in OVLO)		340	450	
I_{SHDN}	Input Shutdown Current	V_{BUS} = 5V, SHDN = HIGH, internal 10MΩ from VBUS to GND		0.5	1	µA
R_{VBUS_SHDN}	Input Resistance in Shutdown	V_{BUS} = 5V, SHDN = HIGH, resistance from VBUS to GND	5	10		MΩ
$V_{IN\_WORKING}$	Input Clamp Working Voltage	Positive Reverse Working Voltage			28	V
		Negative Reverse Working Voltage	-6			
V_{IN_CLAMP}	Input Clamp Breakdown Voltage	I_{IN} = 10mA, T_A = 25°C	30	32	34	V
		I_{IN} = -10mA, T_A = 25°C	-10	-8	-6	
V_{IN_SURGE}	Input Clamp Surge Voltage	+200V surge, T_A = 25°C		38		V
		-200V surge, T_A = 25°C		-6		
V_{BUS_UVLO}	Under Voltage Lockout	V_{BUS} Rising	2.25	2.50	2.75	V
		Hysteresis		100		mV

OVP VBUS to VOUT

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON_VOUT}	On-Resistance VBUS to VOUT	V_{BUS} = 5V, I_{VOUT} = 1A, T_A = 25°C		20	36	mΩ
		V_{BUS} = 12V, I_{VOUT} = 1A, T_A = 25°C		20	36	
		OTG mode, V_{OUT} = 5V, I_{VBUS} = 1A, T_A = 25°C		20	36	
V_{VOUT_OVLO}	Over-Voltage Trip Level	V_{BUS} Rising, T_A = 25°C	13.2	13.9	14.3	V

OVP VBUS to SYS

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON_SYS}	On-Resistance VBUS to SYS	V_{BUS} = 3V, I_{VSYS} = 1A, T_A = 25°C		35	45	mΩ
V_{SYS_OVLO}	Over-Voltage Trip Level	V_{BUS} Rising, T_A = 25°C	5.0	5.25	5.5	V
I_{SYS_RB}	SYS-to-GND Reverse Current	V_{SYS} = 4.4V, V_{BUS} = 0V, T_A = 25°C		0.1	1	µA
I_{VBUS_RB}	SYS-to-VBUS Reverse Current[6]	V_{SYS} = 4.4V, V_{BUS} = 0V, T_A = 25°C, measured at VBUS, no ambient light		75	2000	pA

5. KTS1656 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

6. Guaranteed by characterization and design.

Electrical Characteristics (continue)[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, V_{BUS} = 2.7V to 13.2V. Typical values are specified at room temperature (25°C) with V_{BUS} = 5V, I_{VBUS} ≤ 2A, SHDN = $\overline{EN1}$ = EN2 = LOW, LDO = OPEN, C_{VBUS} = 0.1µF and T_A = 25°C.

LDO

Symbol	Description	Conditions		Min	Typ	Max	Units
LDO	LDO Output Voltage	V_{BUS} = 5V, I_{LDO} = 0mA	T_A = 25°C	3.6	4.0	4.4	V
		V_{BUS} = 15V, I_{LDO} = 0mA		3.6	4.0	4.4	
		V_{BUS} = 5V, I_{LDO} = 100mA		3.6	4.0	4.4	
		V_{BUS} = 15V, I_{LDO} = 100mA		3.6	4.0	4.4	
I_{LK_LDO}	LDO-to-GND Leakage Current	V_{LDO} = 5V, V_{BUS} = 0V, T_A = 25°C			0.01	1	µA
I_{LDO_VBUS}	LDO-to-VBUS Leakage Current[6]	V_{LDO} = 5V, V_{BUS} = 0V, T_A = 25°C, measured at VBUS, no ambient light			50	2000	pA

VBUS Active Discharge (VBUSD)

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{AD}	Active Discharge Resistance (measured from VBUS to GND)	V_{VBUSD}= 3V	115	215	315	Ω
		V_{VBUSD}= 2V		575		Ω
		V_{VBUSD}= 1.5V		1.4		kΩ
		V_{VBUSD}= 1.4V		1.8		kΩ
		V_{VBUSD}= 1.2V, T_A = 0°C to +85°C		3.4	5	kΩ
V_{IH_VBUSD}	VBUSD Input High Voltage	R_{AD} < 5kΩ, T_A = 0°C to +85°C	1.2			V
V_{IL_VBUSD}	VBUSD Input Low Voltage	R_{AD} is high-Z			0.5	V
R_{VBUSD_PD}	VBUSD Internal Pull-Down Resistor			1		MΩ

Digital Signals (FLAG, $\overline{EN1}$, EN2, SHDN)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{FLAG_OH}	FLAG Output HIGH Voltage	V_{BUS} = 5V, EN2 = HIGH	1.65	1.85	2.05	V
V_{FLAG_OL}	FLAG Output LOW Voltage	V_{BUS} = 5V, EN2 = LOW			0.5	V
V_{IH}	Logic Input HIGH Voltage	V_{BUS} = 2.7V to 13.2V	1.2			V
V_{IL}	Logic Input LOW Voltage				0.35	
I_{LK_LOGIC}	Logic Input Leakage Current	V_{BUS} = 5V, VOUT and SYS = Float		5	9	µA
R_{PD}	$\overline{EN1}$, EN2, SHDN Internal Pull-Down Resistor			1		MΩ

Thermal Shutdown[6]

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{J_TH}	IC Junction Thermal Shutdown			150		°C
	IC Junction Thermal Shutdown Hysteresis			20		°C

Electrical Characteristics (continue)[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, V_{BUS} = 2.7V to 13.2V. Typical values are specified at room temperature (25°C) with V_{BUS} = 5V, I_{VBUS} ≤ 2A, SHDN = $\overline{EN1}$ = EN2 = LOW, LDO = OPEN, C_{VBUS} = 0.1µF and T_A = 25°C.

TIMING CHARACTERISTICS (Figures 1-6)

VOUT

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{VOUT_SS}	VOUT Soft-Start Time	Time from V_{BUS} = V_{BUS_UVLO} to 10% of LDO		30		ms
t_{DEB_VOUT}	VOUT Debounce Time	Time from V_{BUS_UVLO} <V_{BUS}<V_{OUT_OVLO} to 10% of V_{OUT}		15		ms
t_{ON_VOUT}	VOUT Switch Turn-on Time	V_{OUT} from 10% of V_{BUS} to 90% of V_{BUS}, R_L = 100Ω, C_L = 22µF		2		ms
t_{OFF_VOUT}	VOUT Switch Turn-off Time[6]	V_{BUS} > V_{OUT_OVLO} to V_{OUT} stop rising, R_L = 100Ω, no C_{OUT}, V_{BUS} = $5V_{DC}$ + $200V_{SURGE}$, T_A = 25°C			100	ns

SYS

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{SYS_SS}	SYS Soft-Start Time	Time from V_{BUS} = V_{BUS_UVLO} to 10% of FLAG		30		ms
t_{DEB_SYS}	SYS Debounce Time	Time from V_{BUS_UVLO} <V_{BUS}<V_{OUT_OVLO} to V_{SYS} rise above 10% of V_{BUS}		15		ms
t_{ON_SYS}	SYS Switch Turn-on Time	Time for V_{SYS} to rise from 10% to 90% of V_{BUS}, R_L = 100Ω, C_L = 22µF		2		ms
t_{OFF_SYS}	SYS Switch Turn-off Time[6]	V_{BUS} > V_{SYS_OVLO} to V_{SYS} stop rising, R_L = 100Ω, no C_{SYS}, V_{BUS} = $5V_{DC}$ + $200V_{SURGE}$, T_A = 25°C			100	ns

VBUS Discharge (VBUSD)

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{VBUS_VBUSD}	VBUS (VBUSD) Discharge Turn-on Time	V_{OUT} = 5V→0V, C_{VBUS} = 1µF, VBUSD= $\overline{EN1}$ = 0V→3V, time for V_{BUS} to fall below 0.8V		600		µs
t_{VBUSD_OFF}	VBUS (VBUSD) Discharge Turn-off Time	V_{OUT} = 5V, C_{VBUS} = 1µF, VBUSD= $\overline{EN1}$ = 3V→0V, time for V_{BUS} to rise to 10% of V_{OUT}		15		ms

OTG

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DON_OTG}	OTG Turn-on Delay (Debounce) Time	V_{OUT} = 5V, C_{VBUS} = 1µF, R_L = 10Ω, $\overline{EN1}$ = HIGH→LOW, time for V_{BUS} to rise above 10% of V_{OUT}		15		ms
t_{ON_OTG}	OTG Turn-on Time	V_{OUT} = 5V, C_{VBUS} = 1µF, R_L = 10Ω, $\overline{EN1}$ = HIGH→LOW, time for V_{BUS} to rise from 10% to 90% of V_{OUT}		300		µs
t_{DOFF_OTG}	OTG Turn-off Delay (Debounce) Time	V_{OUT} = 5V, C_{VBUS} = 1µF, R_L = 1kΩ, $\overline{EN1}$ = LOW→HIGH, time for V_{BUS} to fall below 80% of V_{OUT}		500		µs
t_{OFF_OTG}	OTG Turn-off Time	V_{OUT} = 5V, C_{VBUS} = 1µF, R_L = 1kΩ, $\overline{EN1}$ = LOW→HIGH, time for V_{BUS} to fall from 80% to 10% of V_{OUT}		2		ms

Timing Diagrams

VBUS-to-VOUT

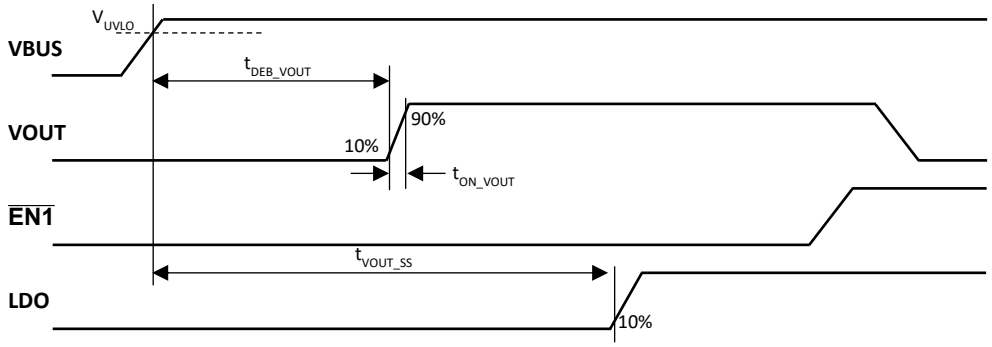


Figure 1. VBUS-to-VOUT Timing Power Up/Down and Normal Operation

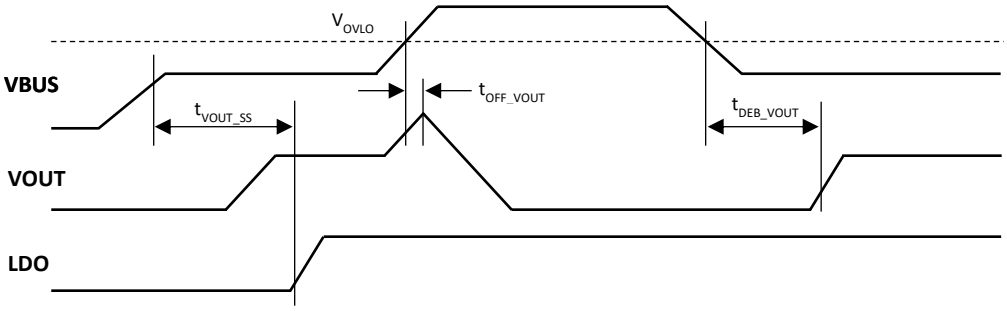


Figure 2. VBUS-to-VOUT Timing OVLO Operation ($\overline{EN1}$ = LOW)

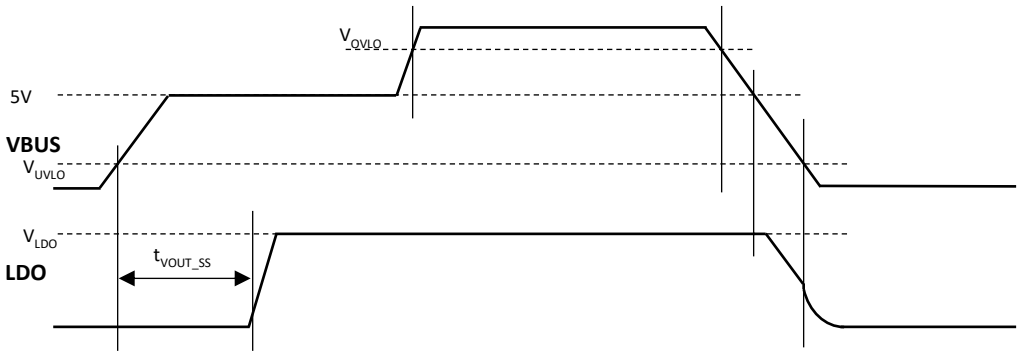


Figure 3. LDO Always-ON Timing ($\overline{EN1}$ = X, EN2 = X, SHDN = LOW)

VBUS-to-SYS

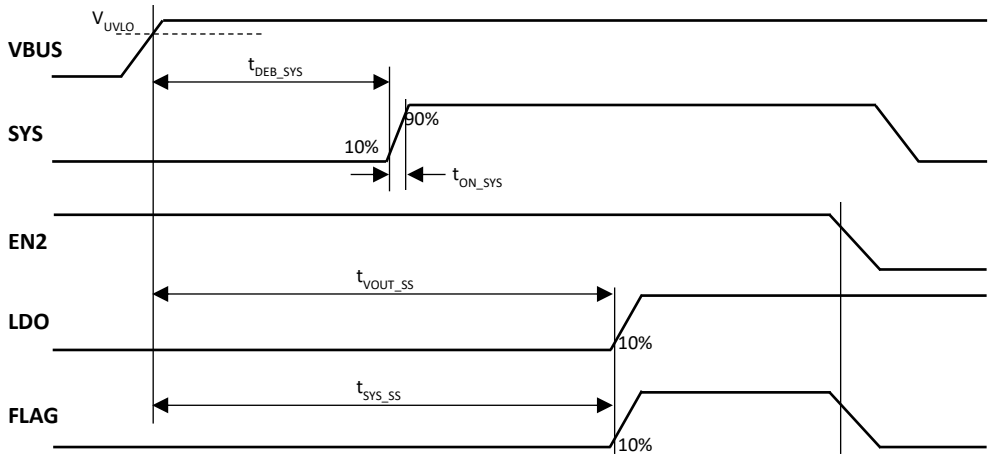


Figure 4. VBUS-to-SYS Timing Power Up/Down and Normal Operation

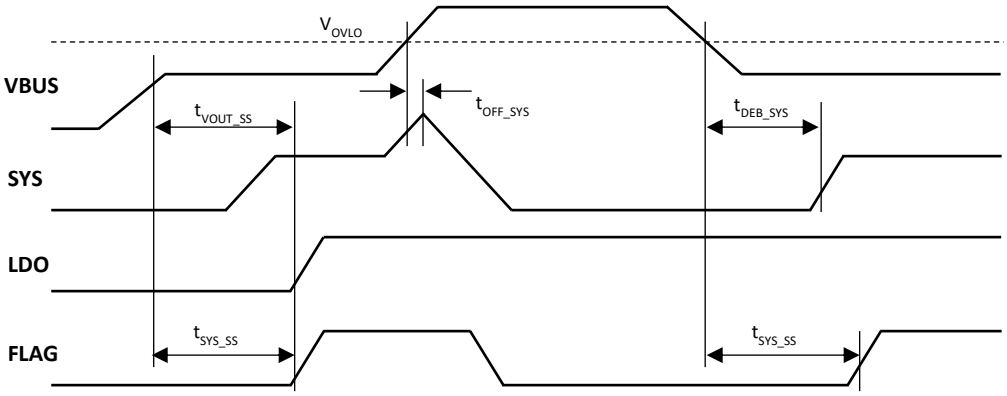


Figure 5. VBUS-to-SYS Timing OVLO Operation (EN2 = HIGH)

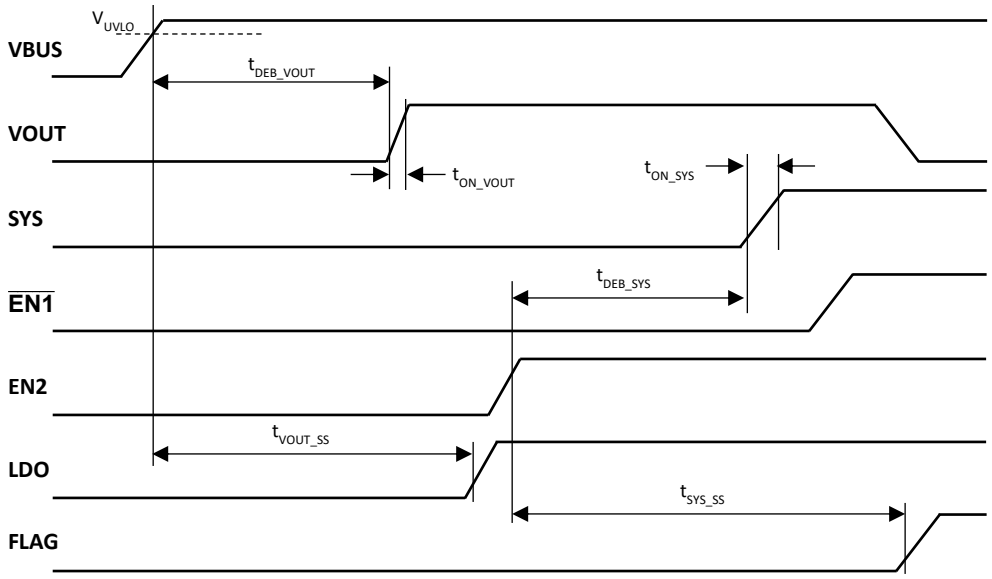
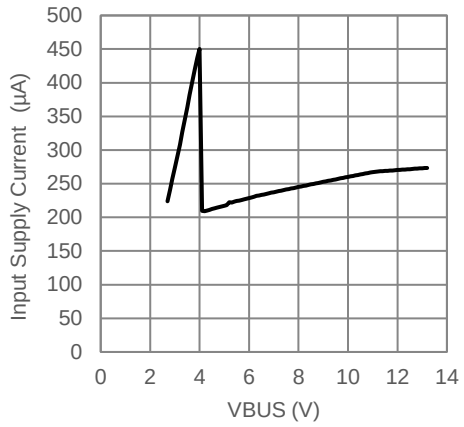


Figure 6. ON/OFF Timing Normal Operation (SHDN = LOW)

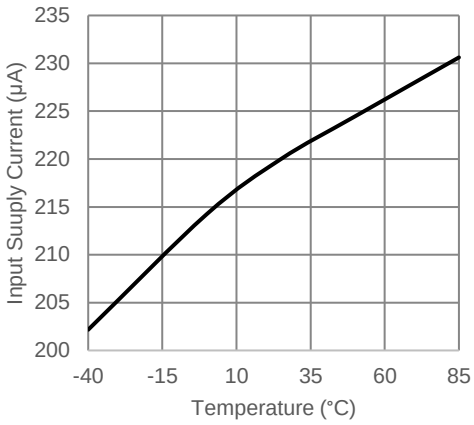
Typical Characteristics

V_{BUS} = 5V, C_{VBUS} = 1µF, C_{VOUT} = 1µF, C_{SYS} = 10µF, C_{LDO} = 4.7µF, T_A = 25°C unless otherwise specified.

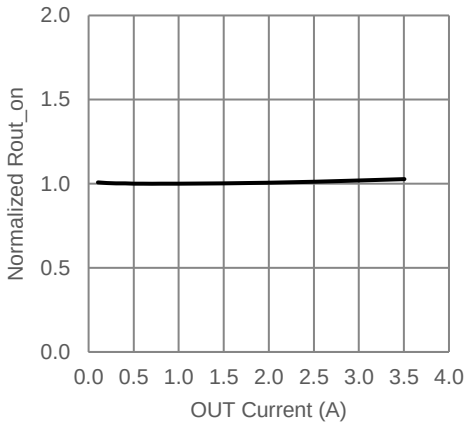
Input Supply Current vs. VBUS Voltage (No Load)



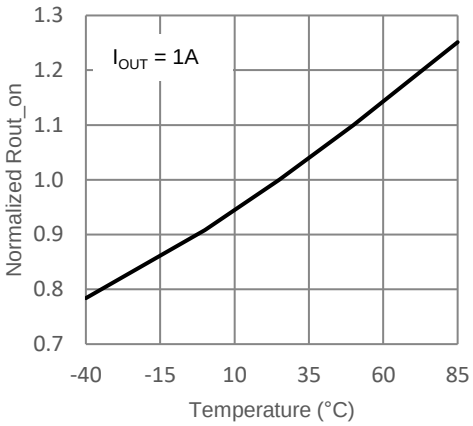
Input Supply Current vs. Temperature



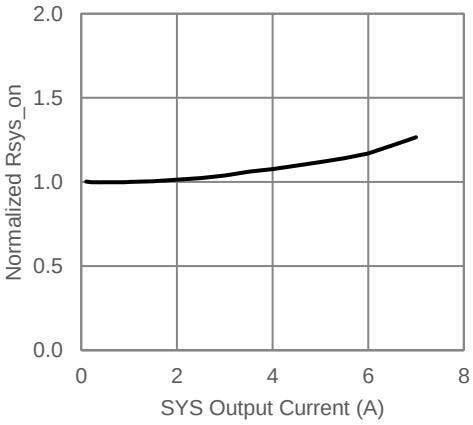
Normalized R_{VOUT_ON} vs Output Current



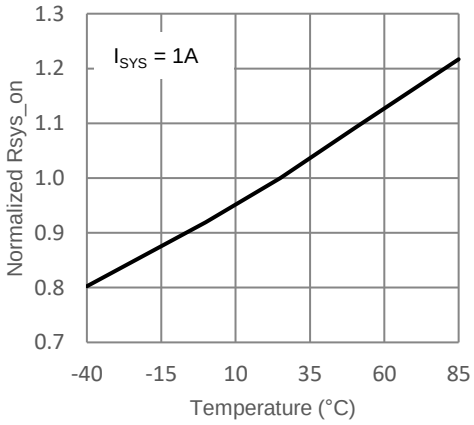
Normalized R_{VOUT_ON} vs. Temperature



Normalized R_{SYS_ON} vs Output Current



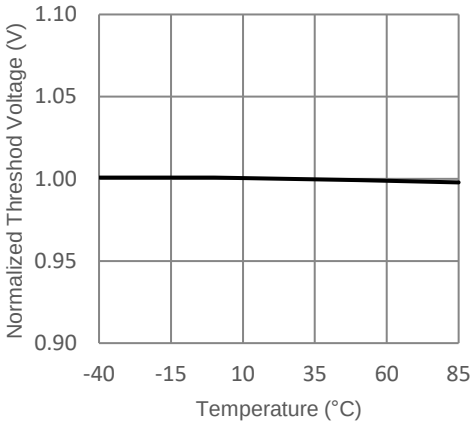
Normalized R_{SYS_ON} vs. Temperature



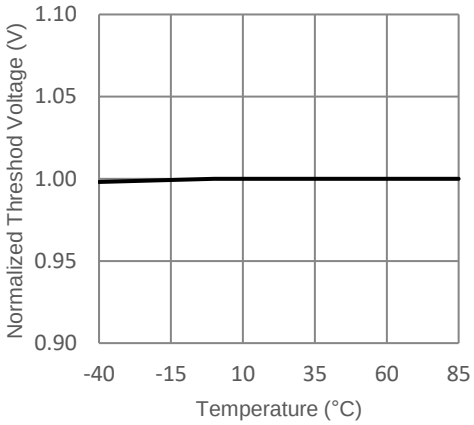
Typical Characteristics (continued)

V_{BUS} = 5V, C_{VBUS} = 1µF, C_{VOUT} = 1µF, C_{SYS} = 10µF, C_{LDO} = 4.7µF, T_A = 25°C unless otherwise specified.

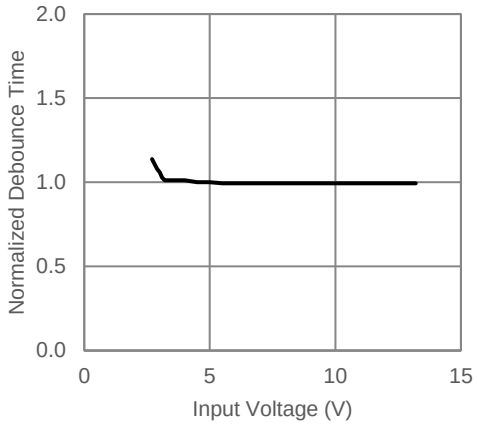
Normalized VOUT OVLO vs Temperature



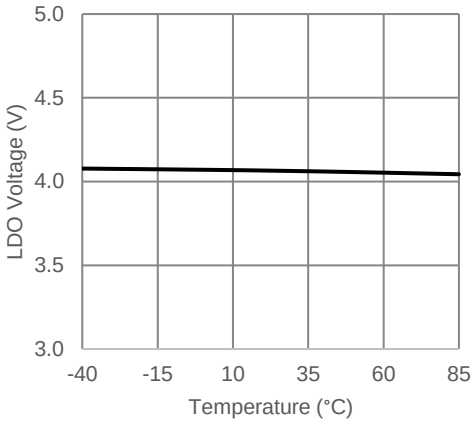
Normalized VSYS OVLO Threshold vs Temperature



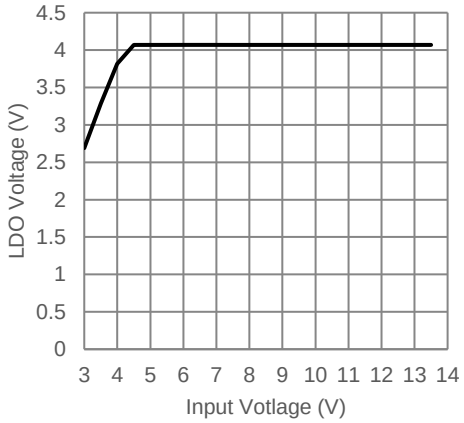
Normalized Debounce Time vs. VBUS



VLDO vs Temperature



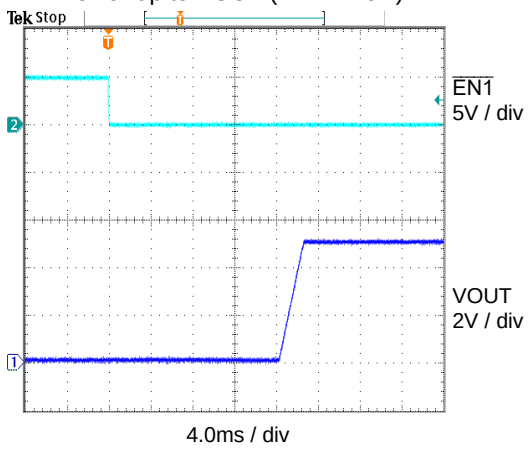
VLDO vs. VBUS (ILDO = 20mA)



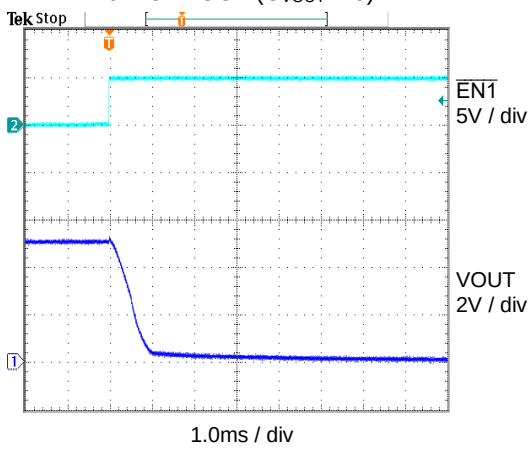
Typical Characteristics (continued)

V_{BUS} = 5V, C_{VBUS} = 1µF, C_{VOUT} = 1µF, C_{SYS} = 10µF, C_{LDO} = 4.7µF, T_A = 25°C unless otherwise specified.

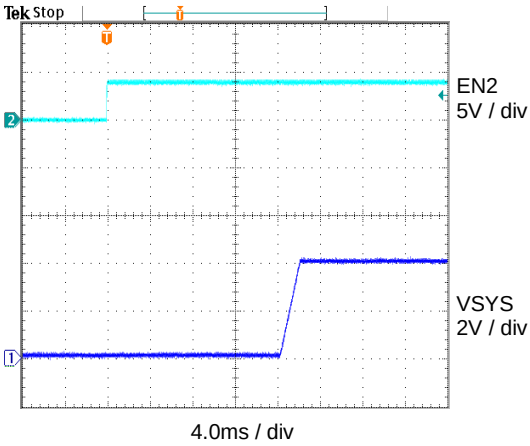
Power-up to VOUT ($\overline{EN1}$ = Low)



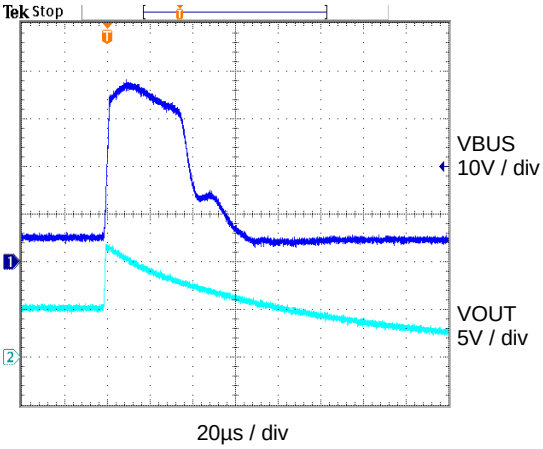
Turn off VOUT (C_{VOUT} = 0)



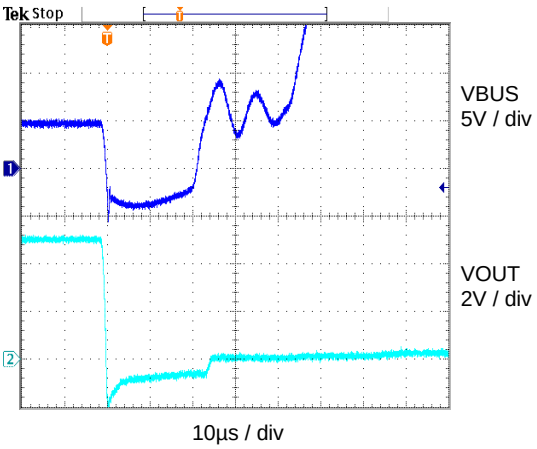
Power-up to VSYS (VBUS = 4V, EN2 = High)



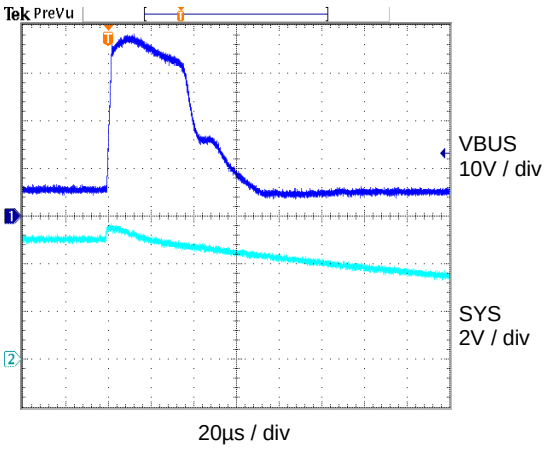
+200V VBUS Surge Transient (VOUT path enabled)



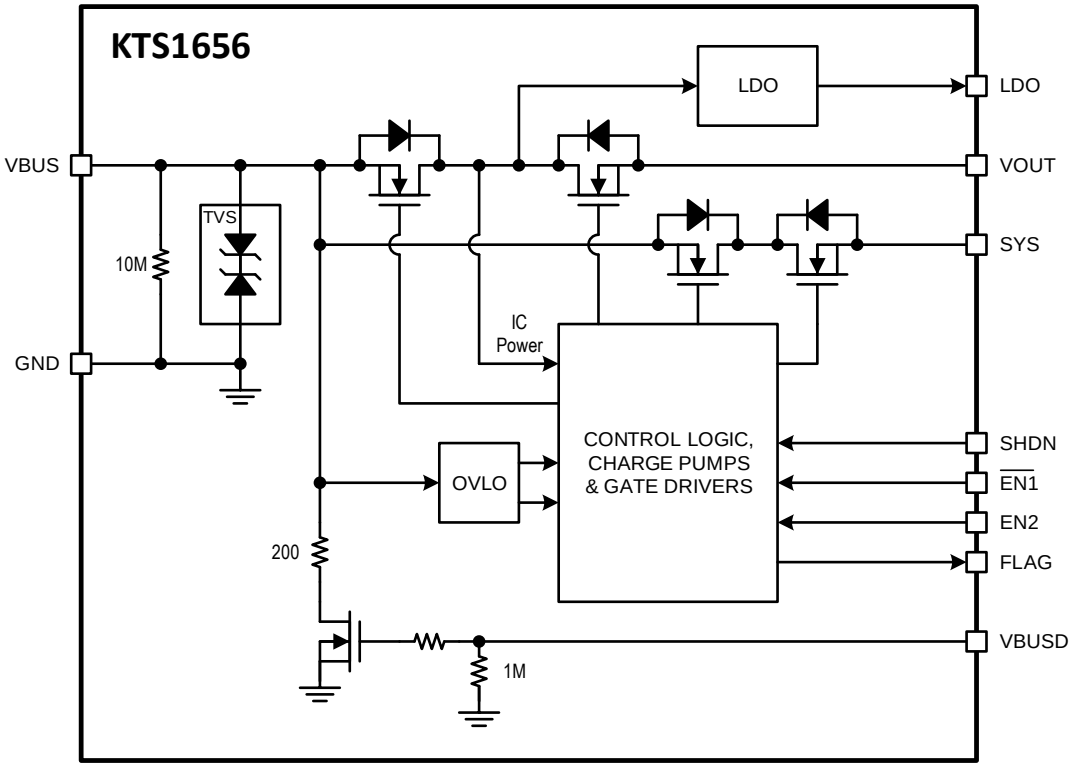
-200V VBUS Surge Transient (VOUT path enabled)



+200V VBUS Surge Transient (SYS path enabled)



Functional Block Diagram



Functional Description

The KTS1656 features two low resistance power switches configured as single input, dual output, change-over switch. The input to both switches is protected against VBUS surge voltages of up to ±200V, and is also protected against over-voltage, with preset trip points on both the VBUS-to-VOUT and VBUS-to-SYS paths, providing protection to downstream components from abnormal input conditions.

The main switch (VBUS to VOUT) features an active–LOW enabled, reverse-blocking 3.5A rated MOSFET, with an OVP trip point of 13.9V. The secondary switch (VBUS to SYS) is an active-HIGH enabled, reverse-blocking 6.0A rated MOSFET, with an OVP trip point of 5.25V. The input to both switches is rated up to a maximum of 28V and minimum of -6V and includes a 15ms debounce time, ensuring that the input VBUS input is stable.

When VBUS is greater than the UVLO of typically 2.5V, the LDO output provides an “always ON” power source, regulated to typically 4.0V, regardless of the status of OVLO, $\overline{EN1}$ and EN2, to power downstream components permitting operation without an installed battery. The LDO can supply up to 100mA of output current.

The KTS1656 can be powered up from VBUS or VOUT to enable operation in systems that support OTG.

The KTS1656 also features an active-HIGH shutdown pin (SHDN) to conserve power, plus over-temperature thermal protection circuitry with hysteresis.

An active HIGH, CMOS FLAG is asserted whenever the SYS switch is active and is in a normal operating mode. The FLAG is de-asserted when the SYS switch is OFF due to either EN2 = LOW, VBUS is in UVLO or OVLO, thermal shutdown or SHDN = HIGH.

The truth table for KTS1656 is shown in Table 1 below.

Table 1. KTS1656 Truth Table

SHDN	$\overline{EN1}$ (VOUT)	EN2 (SYS)	VOUT SW	SYS SW	FLAG	LDO
0	0	0	ON	OFF	LOW	ON
0	1	0	OFF	OFF	LOW	ON
0	0	1	ON	ON	HIGH	ON
0	1	1	OFF	ON	HIGH	ON
1	X	X	OFF	OFF	LOW	OFF

X = Don't Care

For USB Power Delivery, the KTS1656 features an active discharge for the VBUS node. When the VBUSD analog input is driven HIGH, VBUS is discharged from as high as 20V to below 0.8V within 650ms, with sufficient margin for any excess capacitance on VBUS due to the compliance test equipment.

Application Information

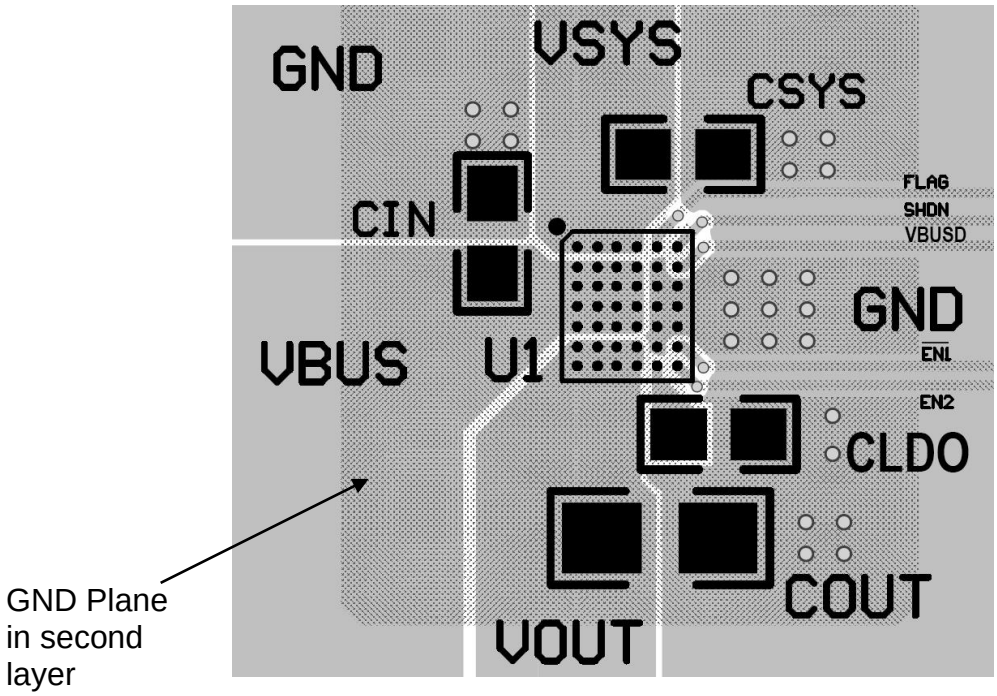
Capacitor Selection

The LDO pin requires a capacitor for stabilizing the internal LDO's operation and storing the charge for load transients. Use a 4.7µF, 10V rated, low ESR, X5R ceramic capacitor for best performance. If the load on LDO is less than 20mA, a 2.2µF ceramic capacitor is sufficient to reduce the solution size.

Capacitors on VBUS, VOUT and SYS supply current for transient load and should be sized according to the transient current requirements. Use X5R ceramic capacitors due to their low variation with temperature and DC bias. Use 1µF or higher for VBUS and VOUT, and 4.7µF or higher for SYS. To avoid over-voltage stress on VBUS's capacitor during surge, use a 50V rated capacitor.

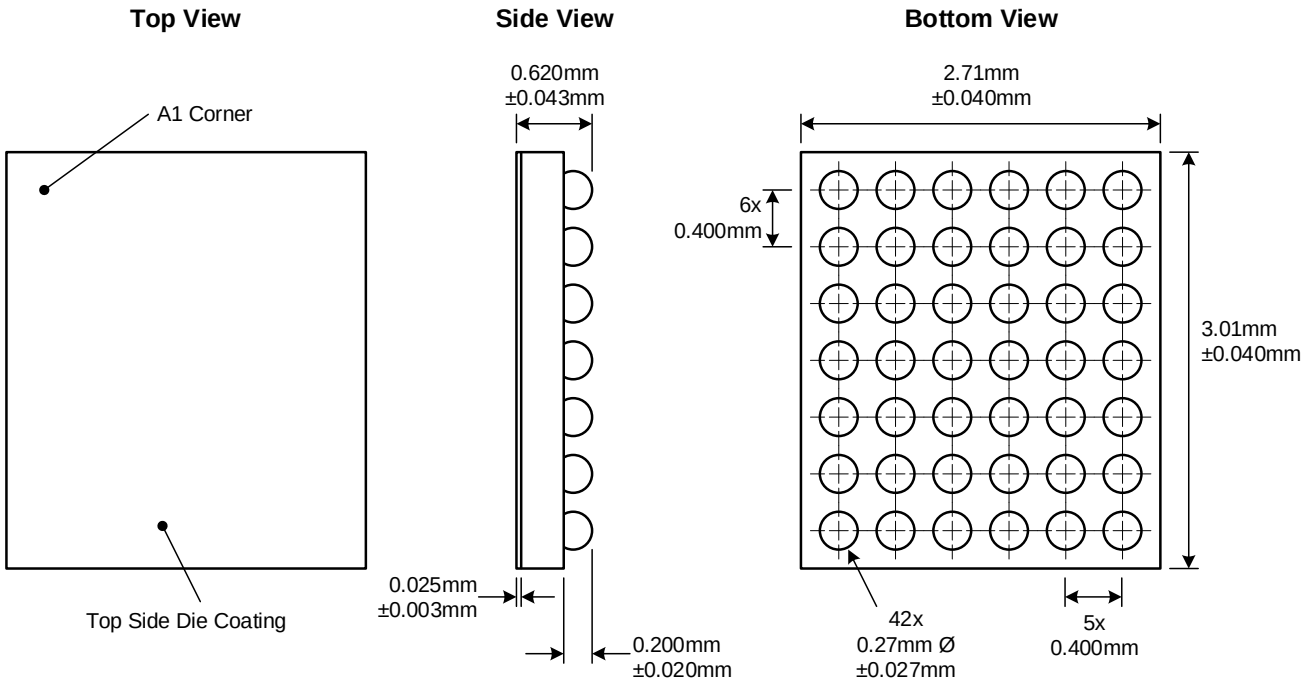
Recommended Layout

It is recommended to place all capacitors close to the IC and the trace length to VBUS, OUT, SYS or LDO pin and the IC GND should be minimized.

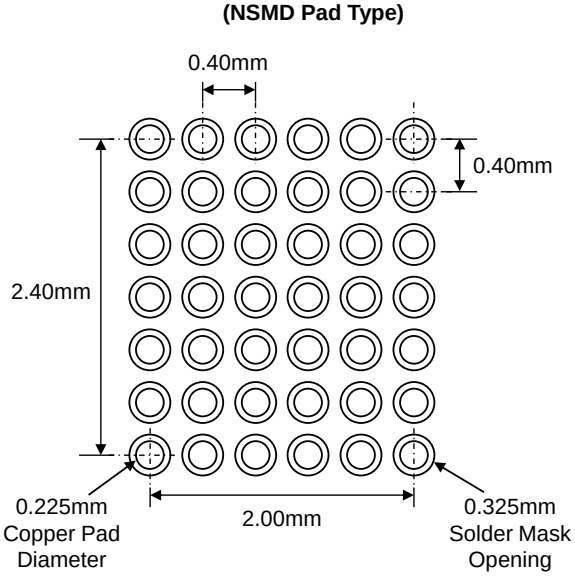


Packaging Information

WLCSP67-42 (2.71mm x 3.01mm x 0.620mm)



Recommended Footprint



* Dimensions are in millimeters.