Application Note AN023

AS1138 Design Guide in Flyback Configuration

Rev 4.0
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FIGURES

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ABOUT APPLICATION NOTE AN023

Application Note AN023 describes the methodology for designing an Kinetic Technologies PD/PWM component into PoE applications using a single-output flyback configuration. This document applies to all flyback designs using the AS1138, even though some diagrams may demonstrate concepts using voltages or power levels specific to only one particular design configuration.

The family of Kinetic AS1138 Flyback Evaluation Boards (EVB) consists of different configurations, including but not limited to the following:

- Regular PoE / local-power inputs of 36-57V
- Low local-power 12V input, plus standard 36-57V PoE input range
- 3.3V output
- 5V output
- 12V output
- Isolated synchronous
- Isolated non-synchronous
- 13W input
- 30W input

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INTRODUCTION

This guide is intended to provide general guidelines for designing with the Kinetic AS1138 Powered Device (PD) Controller & DC-DC Controller in flyback configuration. It is intended to be used in conjunction with the following documents:

- Kinetic Technologies Datasheet:
  AS1138 Datasheet
- Kinetic Technologies Application Note:
  AN006 – Using PoE PD with a Local Power Supply
- Evaluation Boards (containing reference designs):
  AS1138-EV-FL3.3-30W
  AS1138-EV-FL5-30W
  AS1138-EV-FL3.3-30W

It also provides procedures for adapting the reference designs for specific device applications.

For questions or additional information, please contact Kinetic Application Support engineers through your sales representative, or via email at: support@kinet-ic.com.

CIRCUIT DESIGN

PI INTERFACE

IEEE 802.3af/at-compliant systems will use either Alternative A or Alternative B power connectivity. Kinetic recommends that designers adhere to standard IEEE connectivity methodology.

Two external diode bridges are employed to enable connection to the Ethernet RJ45 signals, such that the PD can support any combination of Power Supply Equipment (PSE) polarity and operation mode. Note: IEEE 802.3af/at requires a PD be capable of operation from either Alternative A or Alternative B configurations.

Any qualified PoE Plus (PoE+) transformer or Magjack may be used as the PI interface for 10/100/1000 or 10/100 base Ethernet system connectivity. Ferrite beads L3-L6 in Figure 13 are recommended for impedance matching between the PD and the transformer center taps. Place these components close to the Ethernet transformer/Magjack. If discrete components are to be used, please consult with the Ethernet transformer vendor to ensure that it is PoE+ compatible and that input current will be well balanced between the data lines.

PD SETUP

Current Limit and Classification

RCURR and RCLASS are used for programming PD-compliance levels in the Kinetic AS1138 component.

RCURR sets the on-board current limit. When the pin is left unconnected, current is limited to ≤ 900mA. When connected to ground, the current limit is restricted to ≤ 500mA. Refer to the AS1138 datasheet for specific design limitations.

RCLASS sets the user-programmable classification current level. Each class represents a power-allocation range for a PD, allowing the PSE system to intelligently manage power distribution to each PD that it supports.

Recommended resistance values for the RCLASS pin are listed in Table 1. Refer to the AS1138 Datasheet for more information on resistor selection.

Table 1 - Classification Resistors

Class	Power (Watts)	I_{CLASS}	R_{CLASS}
0	0.44-12.95	0-4 mA	pull-up
1	0.44-3.84	9-12 mA	280k Ω
2	3.84-6.49	17-20 mA	143k Ω
3	6.49-12.95	26-30 mA	90.9k Ω
4	12.96-25.5	36-44 mA	63.4k Ω

Maintain Power Signature (MPS)

For the PD to continually receive power from the PSE, it must maintain its power signature so the PSE continues to see a valid load profile. For more info on MPS, please refer to Appendix A of Application Note AN006 – Using PoE Powered Devices with a Local Power Supply.

ISOLATED FLYBACK DC-DC CONVERTER DESIGN TECHNIQUES

The AS1138 supports isolated forward, flyback and non-isolated buck DC-DC topologies. Information on the different topologies can be found in the AS1138 datasheet.

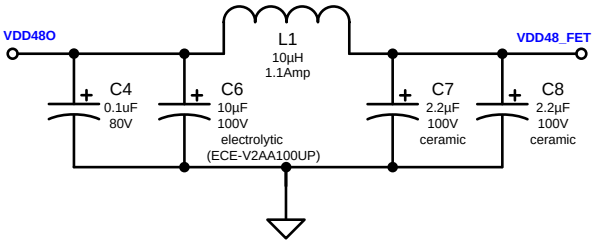
Designers must also decide whether or not their architecture requires power isolation. If the system will be non-isolated, then the input and output grounds should be connected together.

If the system will be isolated, then an opto-coupler is required on the feedback line to ensure that no DC path connects the two sides of the circuit. To reduce common-mode noise on the Ethernet lines, a 4700pF, 2KV cap is recommended between PoE ground and board ground.

Input Noise Filter at VDD48O

A pi-type filter should be employed on the VDD48O pin, to reduce the amount of noise on the line. The following filter is recommended between the PD VDD48O pin and the transformer primary-winding node:

Figure 1 - Pi-Type Filter

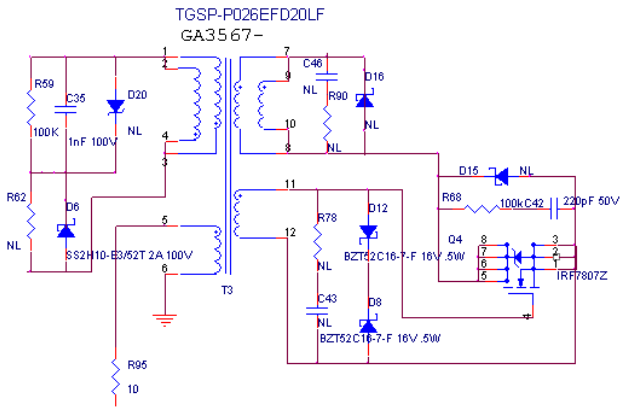


In addition, designers must ensure that any device connected to VDD48O be rated to safely handle at least 80V and >1A.

Snubbing Circuit Design

The most common snubbing circuit is the series R/C, which is placed as close as practical across the device being protected. The R/C time constant of the circuit should be small in comparison to the switching period, but long relative to the voltage rise time. The capacitor must be larger than the parasitic capacitance, but as small as possible, to minimize power dissipation through the snubbing resistor.

Figure 2 - Snubbing Circuits Used in AS1138 Flyback EVB



There are three snubbing circuits used in the AS1138 reference design shown in Figure 2. One snubbing circuit consists of R59, C35, R62, D6 and D20. Normally, resistor R62 is not installed. If R62 is to be employed, then do not place a resistor in R59. Another snubbing circuit is comprised of R78, C43, D12 and D8. The third snubbing circuit example contains C46, R90 and D16.

In designing an AS1138 snubbing circuit, designers should begin by measuring the frequency of the ring without the snubbing circuit in place, then begin circuit tuning by adding a small capacitor (in the 100pF range) across the device and again observing the ring. Then, increase the capacitance until the ring is roughly halved and note the capacitor value. The actual capacitor to be used in the design will be 75% of the capacitance value just determined.

Add a 25ohm resistor in series with this capacitor and then keep increasing the resistance until the ring is nearly eliminated. Capacitors should be the ceramic type, which have low ESR and ESL properties. Avoid wire-wound resistors, which have excessively high ESL.

Another design consideration is the sync winding, which is used to drive the Synchronization FET. Usually a bi-directional TVS diode is used to clamp the winding voltage to a safe level for the VGS = 20V rating of most FETs. A 16V rated part is ideal for most applications.

The benefit of a TVS diode circuit over an R/C snubber or a gate-drive resistor is that the switching time is not affected, minimizing overlap losses. In some cases, however, a gate-drive resistor or snubber may be required. Designers should experiment to determine the optimal solution for their application.

Adding a snubbing circuit to minimize spikes and ringing can be beneficial for device protection and EMI, but the undesirable effect is reduced efficiency. Care must be taken in selecting these components and observing the effects. Board layout plays a significant role in circuit performance, along with transformer parasitics.

Besides the snubbing circuit, in the AS1138 reference designs, various EMI suppression techniques are implemented as backup solutions whenever needed. For example:

- Resistor R57 can be used to slow down the rising edge of the primary switching FET.
- Resistor R77 (not shown in Figure 2) can be added into the design between pin 11 of transformer T3 and the gate of Q4 to reduce spike stretches on the Sync FET for better EMI performance (for 5-10ohm).

Since lab test results show that Kinetic EVB EMI emissions are already well controlled, resistors R57 and R77 are populated with zero-ohm resistors.

Synchronization FET Selection

In general, adding a synchronization (sync) circuit, improves the DC-DC converter efficiency by a few percent. However, care must be taken when selecting the sync FET component. The major parameters important to circuit efficiency are the drain to source resistance, the rise/fall times and the total gate charge.

RDS_{ON} value should be in the 8-16 mΩ range. FET rise/fall times should be approximately 10ns. The important parameters to prevent FET component stress are the maximum drain to source voltage and the maximum gate to source voltage. Under no-load or light-load conditions, the peak voltage across the drain-to-source might exceed the V_{DS} rating of the FET. System designers should tune the transformer turns ratio to minimize this stress. It is the designer's responsibility to assure that FET and circuit parameters are not exceeded.

Kinetic recommended reference designs, including the recommended transformers and sync FET, have been optimized to keep node voltages around the sync FET within their desirable ranges, to avoid overstressing components.

Control-loop Stability vs. Crossover Frequency Tuning

A conventional optically-isolated error op-amp is used to compensate for control-loop stability. The system control loop shown in Figure 3 and Figure 4 has two poles, P1 and P2, and one zero, Z1, to compensate the loop.

Pole P1 is formed by AEA - the DC gain and capacitor C21. Pole P2 is created by the equivalent output capacitor and load resistor. The zero is formed from feedback compensation resistor R56 and capacitor C21.

An additional zero Z2 and pole P3 may be optionally employed for added phase margin and to cancel high-frequency noise, if required. The extra pole and zero are formed from capacitors C22 and C27 and resistor R26.

Figure 3 - Control Loop Section at the Output

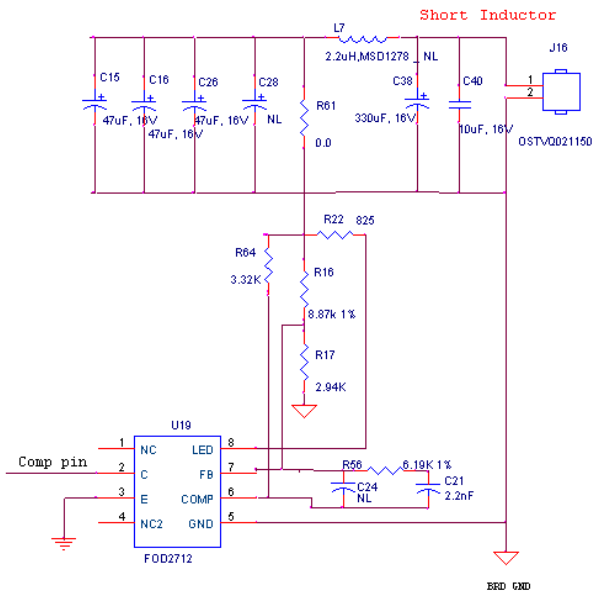
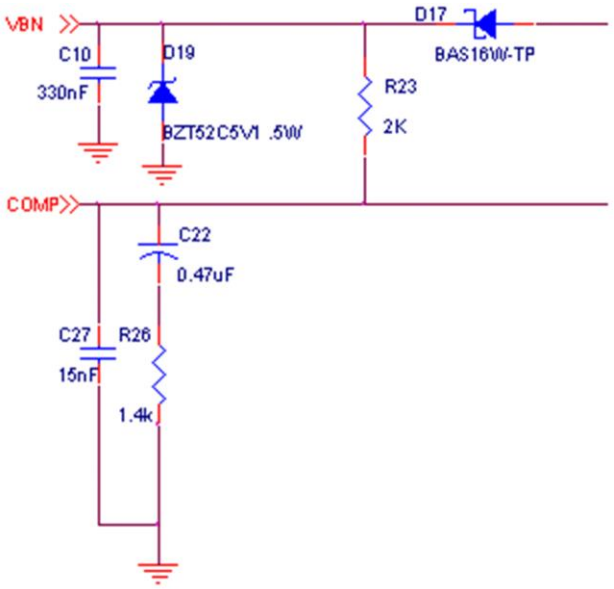


Figure 4 - Control-loop Section Close to the DC-DC Controller



Poles and zeros are calculated with these equations:

$$R_{LOAD} = \frac{V_{OUT}}{I_{MAX}}$$

$$N = \frac{N_{PRIMARY}}{N_{SECONDARY}}$$

$$D = \frac{N \cdot V_{OUT}}{(V_{IN} + N \cdot V_{OUT})}$$

$$f_{P1} = AEA \cdot \frac{1}{(2\pi \cdot C21)}$$

$$f_{P2} = \frac{1}{(2\pi \cdot C_{OUT} \cdot R_{LOAD})}$$

$$f_{Z1} = \frac{1}{(2\pi \cdot C21 \cdot R56)}$$

The additional pole and zero are calculated using:

$$f_{P3} = \frac{1}{(2\pi \cdot C27 \cdot R26)}$$

$$f_{Z2} = \frac{1}{(2\pi \cdot C22 \cdot R26)}$$

Selecting appropriate component values for pole and zero positions is the key to achieving the desired high DC gain, phase margin, gain margin and gain crossover frequency that is the hallmark of a stable system.

The general rule of thumb is to set pole P1 at the gain crossover frequency, which will determine the value for capacitor C21. The gain crossover frequency must be less than one-sixth of the switching frequency (F_{SW}). Then, set zero Z1 at pole P2.

The optional zero Z2 and pole P3 can be implemented if the system still requires additional phase and higher DC gain for better load regulation. When the zero associated with the output capacitor ESR (Equivalent Series Resistance) is less than one half of F_{SW}, this additional pole and zero can be used to compensate for or minimize the effect caused by the ESR.

Note: Once the additional pole and zero are employed in the design, zero Z2 must be set at pole P2. Zero Z1 will be set farther out at 10*P2. Set P3 equal to the zero of the ESR (Z_{ESR}), using the calculation:

$$f_{ZESR} = \frac{1}{(2\pi \cdot C_{OUT} \cdot R_{ESR})}$$

One further issue designers should pay attention to in flyback designs is the Right Half Plan Zero (RHPZ), which can be found using the following formula:

$$Z_{RHP} = \frac{R_{LOAD} \cdot (1-D)^2 \cdot N^2}{(2\pi \cdot L_P \cdot D)}$$ where:

- R_{LOAD} is the load resistor
- D is the duty cycle.
- N is the turns ratio of primary to secondary
- L_P is the primary inductance of the transformer.

To minimize the effect of Right Half Plan Zero, the gain crossover frequency F_C should be also set to less than one-third of the RHPZ frequency.

Additional output filter inductor L7 may be employed, based on the design's low output ripple and clean no/full load transient response requirements. Use of this inductor changes the impedance of the load seen by the DC-DC control loop and will require appropriate adjustments to the compensation-loop components. Also, if applications require different output capacitance than is specified in the Kinetic reference designs, loop compensation is affected and appropriate component tweaks will be required, using the preceding design guidelines.

Loop stability testing to generate Bode plots can be performed with a traditional small-signal test setup. Transient load-step response should also be checked, to ensure that the transient behavior matches the measured AC-loop parameters.

Please consult with Kinetic' Application Support engineers for further assistance and proper component selection.

Opto-Coupler Biasing

U19 is an 8-pin, optically-isolated Error-Amplifier IC containing an error amplifier and opto-coupler (see Figure 3 and Figure 4).

In order to function properly, the LED voltage at pin 8 should be greater than 2.74V and the current-transfer ratio (I_C/I_F) should be set within the minimum and maximum current-transfer ratio (CTR) over the system's operating temperature range.

The following equations can be used to calculate the opto-coupler bias resistor values:

$$R22 = \frac{(V_{OUT} - V_{LED})}{I_F}$$

$$R23 = \frac{(V_{BN} - V_{COMP})}{I_C}$$

$$R64 = \frac{(V_{OUT} - V_{REF})}{I_{SCOMP}}$$

- I_C/I_F is the current transfer ratio
- I_F is the LED current set by R22
- I_C is the collector current set by R23
- I_{SCOMP} is the current flow into the error amplifier compensation pin 6 of U19.
- Kinetic-recommended voltage levels: V_{LED} = 2.74V, V_{COMP} = 1.8V, V_{REF} = 1.24V.

In general, LED current I_F is set between 2mA and 3mA, to reduce power dissipation and extend the life of the opto-coupler. R64 is used to supply 1-2mA into the error amplifier, to minimize CTR variation over the entire temperature range.

Soft Start and Short-Circuit Protection

The Soft Start function is enabled by grounding the CSS pin through a capacitor, as specified in the Electrical Characteristics table in the AS1138 Datasheet (Soft Start Ramp Time).

During over current faults the IC operates in hic-cup mode to limit the average output current. Since the controller operates in peak current mode control, the peak primary current is limited to the peak current limit threshold defined in the datasheet. Once the peak current limit threshold is exceeded the controller counts 32 consecutive switching (clock) cycles and then shuts down for 256. The sequence repeats until the over current condition is corrected. The over current threshold must be exceeded for all 32 consecutive cycles. Otherwise the counter is reset on the first missed switching cycle and shutdown will not occur. The behavior ensures the converter does not operate in hic-cup mode unless there is a hard over current condition. For light over current condition the peak current mode control limits current.

LV Mode Network vs. Input Voltage

There are still a number of applications that require local power delivery for redundancy or when Ethernet connections at the site are not PoE-capable.

By providing for the use of a wall power adapter, users have the ability to deploy the same equipment in both PoE and non-PoE environments. This also provides a ready migration path when PoE is installed later on.

Diode D13 (see Figure 12 on page 17) is used to block a reversing current from VDD48O. Its maximum leakage current should be specified to be less than 350µA. Local power cabling can cause EMI problems, so appropriate choke/filtering components should be used to isolate the local power jack.

Refer to the AS1138 Datasheet and Application Note AN006 – Using PoE Powered Devices with a Local Power Supply for proper local-voltage mode network setup.

Power Transformer Selection

For the regular PoE input voltage, the transformer selection can be relatively easy and the recommended vendors can provide the support needed in the most cases. However, if the local source voltage is significantly lower than the PoE line (<32V), then special consideration must be taken in the transformer circuit design.

Refer to AN006 – Using PoE Powered Devices with a Local Power Supply for a list of qualified power transformers used in different configurations.
Kinetic has a selection of recommended transformers from leading magnetic suppliers that have been tested for proper circuit performance. Kinetic highly recommends adhering to Kinetic-proven transformer designs for optimal system cost and performance, and to minimize the need for design re-optimization and validation.

COMPONENT PLACEMENT

Component selection and layout placement is very important for good EMI, efficiency and output ripple performance. Appendix A provides example evaluation board schematics for a power splitter design with an isolated flyback DC-DC converter. Example layouts from this board are also provided, to illustrate desirable design and layout practices.

As an additional precaution against EMI and to increase ESD protection, the Kinetic KTA1550 or KTA1552 can be used. Please see the respective data sheets plus application notes AN063, AN065 and AN060 for more information.

ETHERNET SIGNALS

No special placement consideration is required for the Ethernet line components when designing with the AS1138; however, the PD device should be placed as close to the center tap of the transformer as possible, to limit the IR drop.

DC-DC CONVERTER

When using flyback topology, the NDRV FET and its associated protection diodes should be placed as close as practical to the PD/PWM Controller component. Ideally, place them on the reverse side of the board, underneath the PD/PWM Controller. The DC-DC transformer should be placed on the top side of the board, to limit the distance between the switching FETs and the transformer.

Ceramic bypass capacitor C10 should be placed as close as possible to the PD/PWM Controller for optimum sourcing of the switching current from the gate drive of the power FET. This will assist in minimizing high-frequency ringing and ripple at the VBN pin of the AS1138 component. The same applies for decoupling capacitors C1 and C11.

Snubber circuits should be placed very close to the primary or secondary FET where snubbing is required. They may be placed on the back side of the FETs, as appropriate.

When placing components on both sides of the PCB, thermal issues should be carefully considered. All active components in the design (AS1138, FETs, diodes, etc.) require careful layout and ground plane connectivity for thermal management. To minimize the board's thermal density and localized heating, no two active components should be placed back-to-back on opposite sides of the board.

The placement of the 2KV capacitors C13 and C14 is critical for proper EMI performance. It is recommended that one be placed on each side of transformer T3, to allow for design flexibility during testing.

COMPONENT PLACEMENT EXAMPLE

Figure 5 and Figure 6 show example component placements for the top and bottom of a PC board:

Figure 5 - Top-Side Component Placement

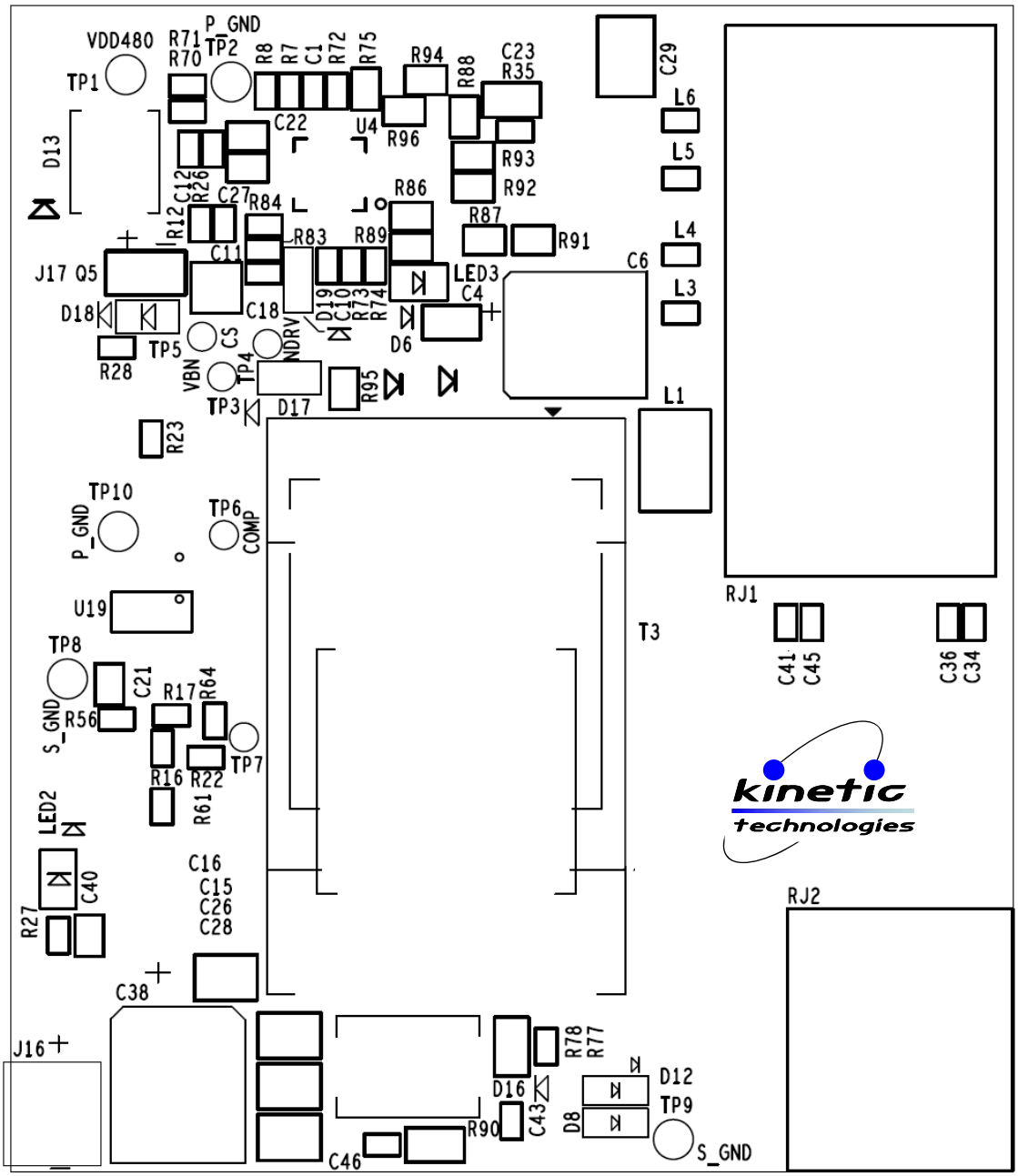
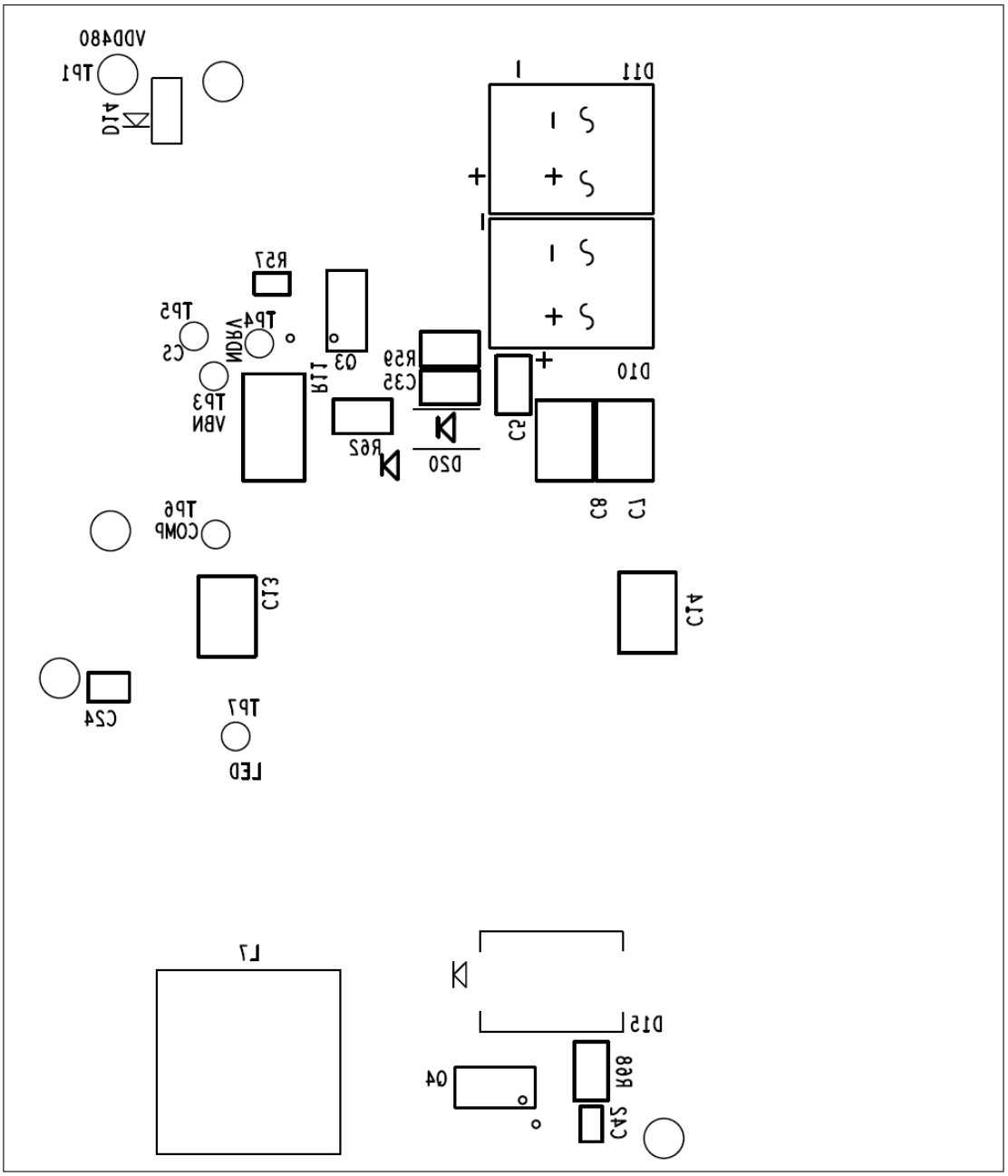


Figure 6 - Bottom-Side Component Placement



ROUTING

ETHERNET SIGNALS

Ethernet signal routing on the secondary side of the input transformer should follow the recommendations of the Ethernet PHY supplier. The AS1138 does not require additional consideration.

In general, Ethernet data signals are high-frequency differential signaling channels. Their routing should have 100ohm differential impedance on both sides of the inputs to the Ethernet transformer. Signal traces should avoid sharp bends and sudden width changes, since this affects impedance and current carrying capacity. Traces should also have appropriate ground planes underneath, for common-mode signal return and to shield against coupled noise from the DC-DC converter.

High-speed signals should be routed away from the DC-DC converter, to prevent the converter switching noise from appearing on the data lines.

Since the Ethernet transformer center-tap connections do not carry data traffic, these traces should be drawn wider on the circuit board to minimize the IR drop due to the relatively large current (up to 1A) to and from the line. The increased width is also recommended in order to carry this current without excessive heating.

Ground planes should be solid and free of islands and choke points, to ensure a low-impedance return path.

DC-DC CONVERTER

VDD48O signal routing should be at least 200mils wide and all components directly connected to it should also be 200mils, including the routing to the drain and gate of the FET between the NDRV and the primary side of the transformer.

Traces leading from the secondary side of the DC-DC converter should be appropriate for the output current of the converter. For maximum power delivery, it is also recommended that a minimum 200mil line width be used. Any layer transitions for these high-power signals require multiple vias to ensure low inductance and resistance. The length of all high-impedance small signal traces should be kept to a minimum and shielded from the switching power traces.

The AS1138's thermal pad should be tied directly to the return of C7 and C8, in a path that will not share the high-power current associated with the DC-DC converter.

Minimizing the loop area for all high-frequency switching currents helps reduce radiated EMI. Ceramic capacitors C7 and C8 supply the high-frequency switching current for the primary side of the integrated converter block in the PD Controller. The loop area made by C7 and C8 with the return path tying to the current-sense resistor R11 should be minimized.

THERMAL PAD

The Kinetic-recommended 5x5mm 20-LD QFN footprint for the AS1138 package should be followed. It is essential that the bottom-side pad be used for both thermal and electrical contact. A good solder connection is essential for optimal performance. This pad should be filled with as many vias as is practical, to ensure good thermal conductivity to the board's ground plane.

It is also recommended that a metal pad be placed on the bottom side of the board. Avoid routing signals underneath. A minimum of nine vias on the ground/thermal pad is required. For additional information, refer to Application Note AN018 – Thermal Characterization & QFN Layout Guide and AN022 – AS1138 Thermal Characterization Report.

STACK-UP AND GENERAL LAYOUT GUIDELINES

For a multilayer board, ground and signal layers should be internal layers, with 1oz copper pour on both the top and bottom layers. Stitch the copper pour areas with ground layers of no greater than 7mm pitch, to avoid islands. This will help with thermal conduction, EMI emission and immunity. Separate active signal layers, both to ensure good capacitance between the layers and to ensure there is a solid reference or return for the active signals.

GROUND LAYERS

The DC-DC converter creates voltages isolated from the high-voltage signals coming in from the Ethernet line. For this reason, two grounds are designed into the system, one for high voltage and one for low voltage.

Grounds should be separated by a gap on the power and ground planes, to reduce DC-DC noise coupling to the Ethernet signals. Kinetic recommends a minimum gap of 50mils. Ground planes should be 1oz copper and should be as continuous as possible, with no isolated islands or narrow choke points.

To maintain ground separation, secondary-side components and routing should be placed over the low-voltage ground plane. Primary-side components and routing should be placed over the high-voltage ground plane.

Maintain sufficient spacing between the traces leading to the power transformer, as well as between the traces from the transformer to other components on the board, to avoid isolation-related issues.

For EMI consideration, Kinetic recommends not filling in the ground plane under the power transformer, as shown in the layout example. This reduces the coupling of switching events from the magnetic transformer to the ground plane. The high voltage/PoE ground should be treated as an island covered by the low-voltage ground, as shown in Figure 9. Via stitching should be used on the outer edges of the board, to ensure low-impedance connectivity between the layers.

LAYOUT EXAMPLE

Figure 7 to Figure 11 are example layouts that apply to the AS1138. Appendix A has corresponding schematics for the implementation of a synchronized flyback-isolated converter.

Note that these designs include footprints and place holders for a wide range of components, to allow Kinetic to modify the design to meet various power, voltage and feature requirements. An application-specific design may be somewhat simplified based on the designer's specific requirements.

Figure 7 - Layout Example – Top Assembly

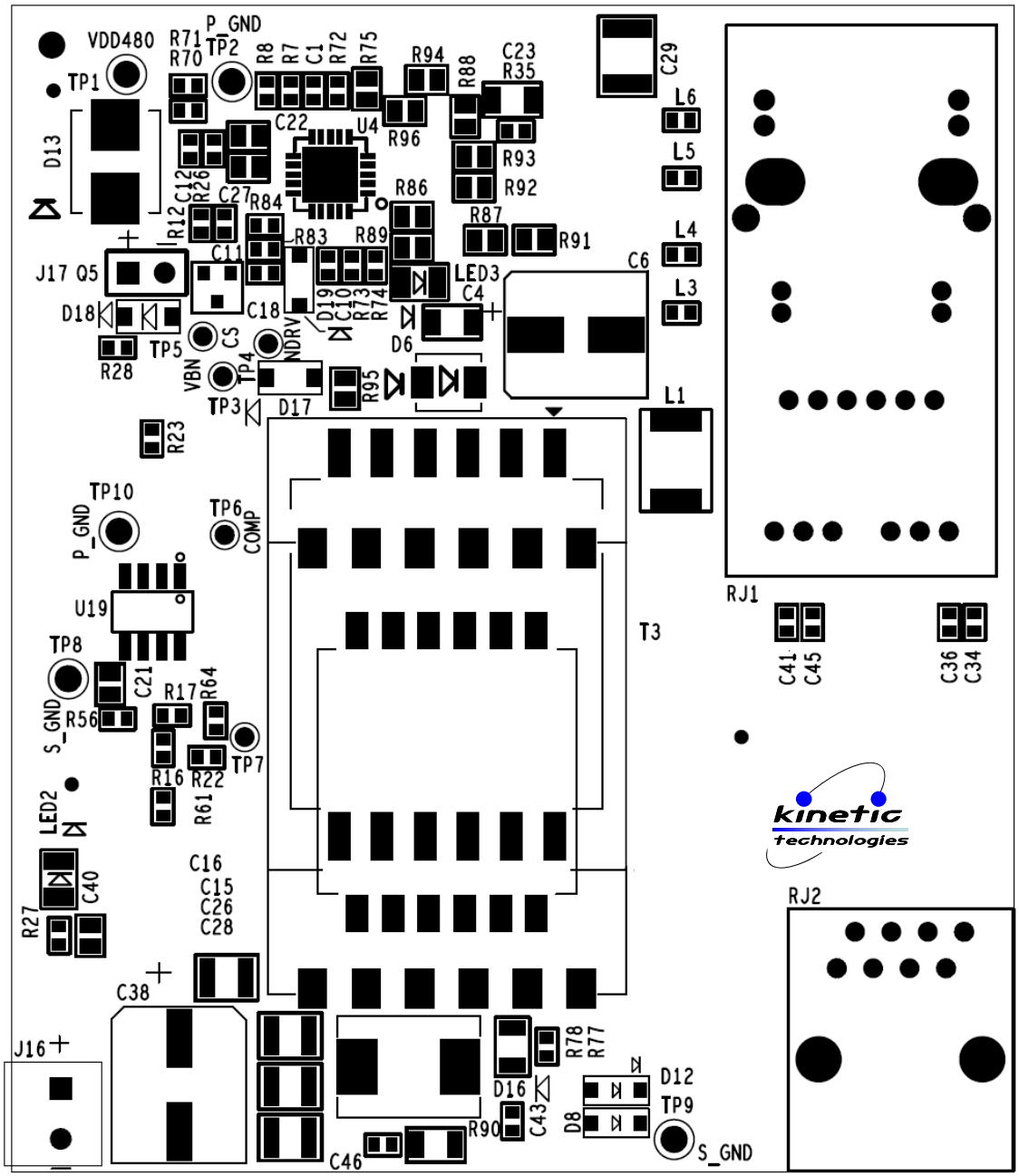


Figure 8 - Layout Example – Top Layer

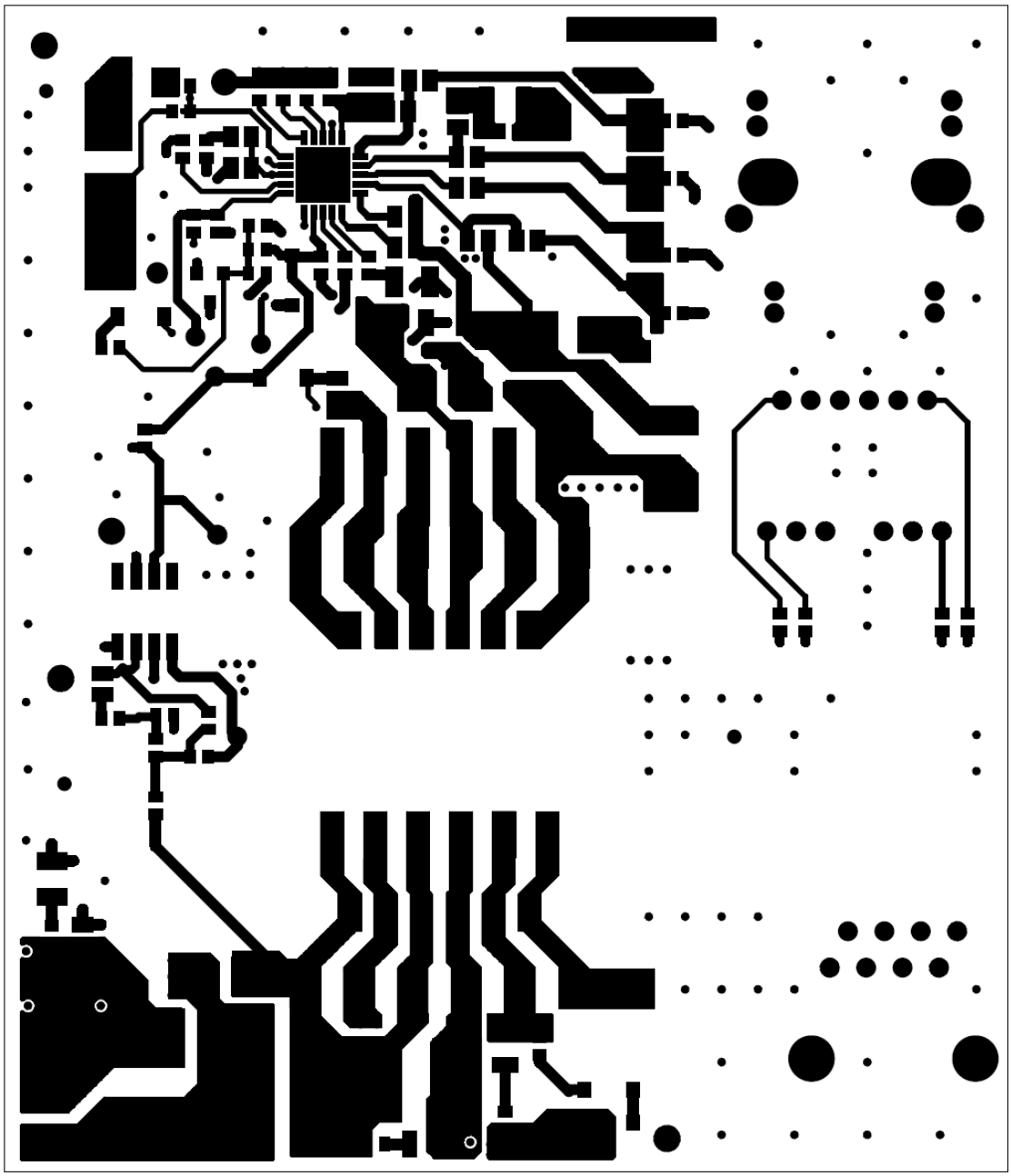


Figure 9 - Recommended Ground Plane Split using Magjack – Shown in Ground Layers 1, 2 and 3

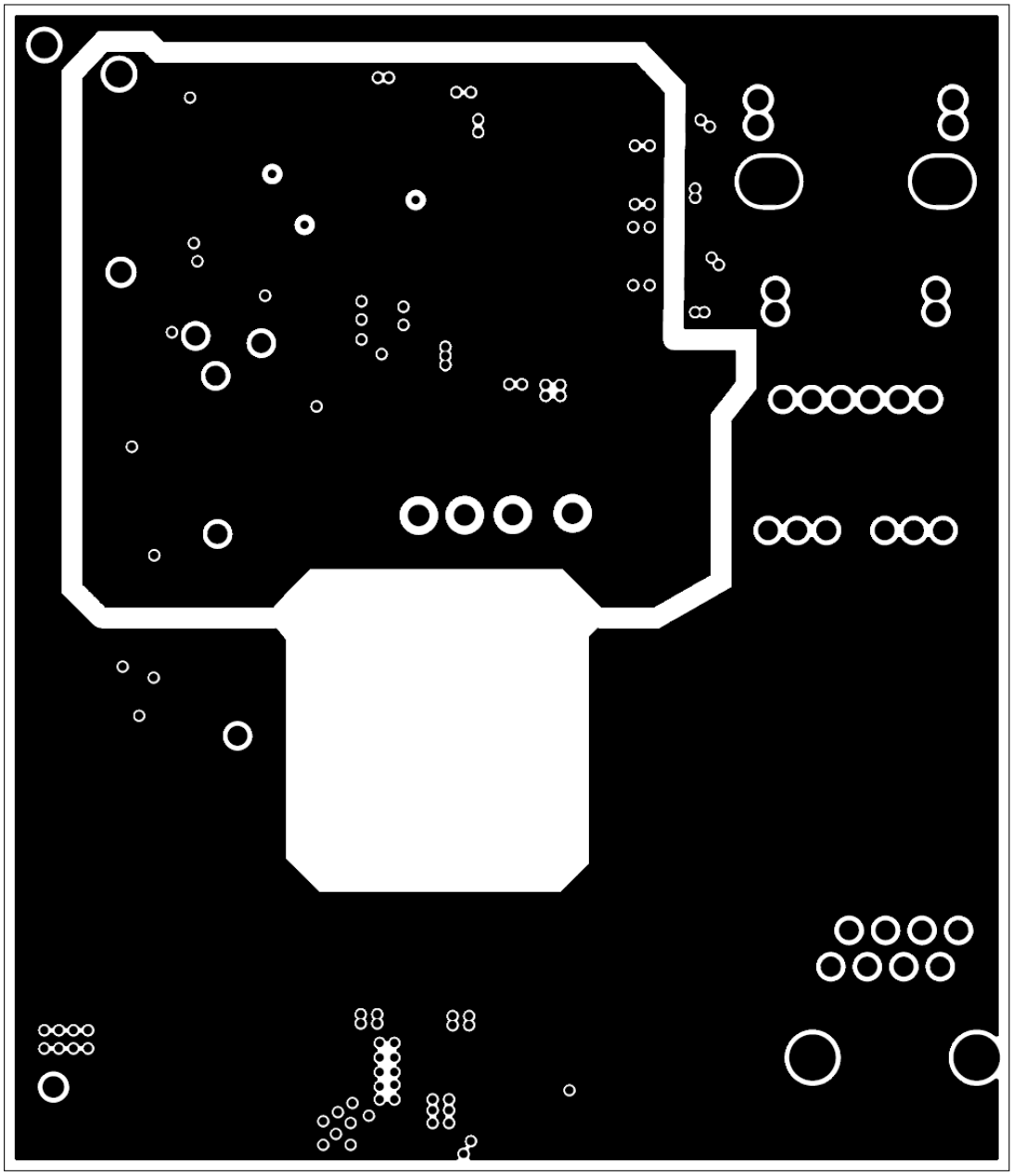


Figure 10 - Layout Example – Bottom Layer

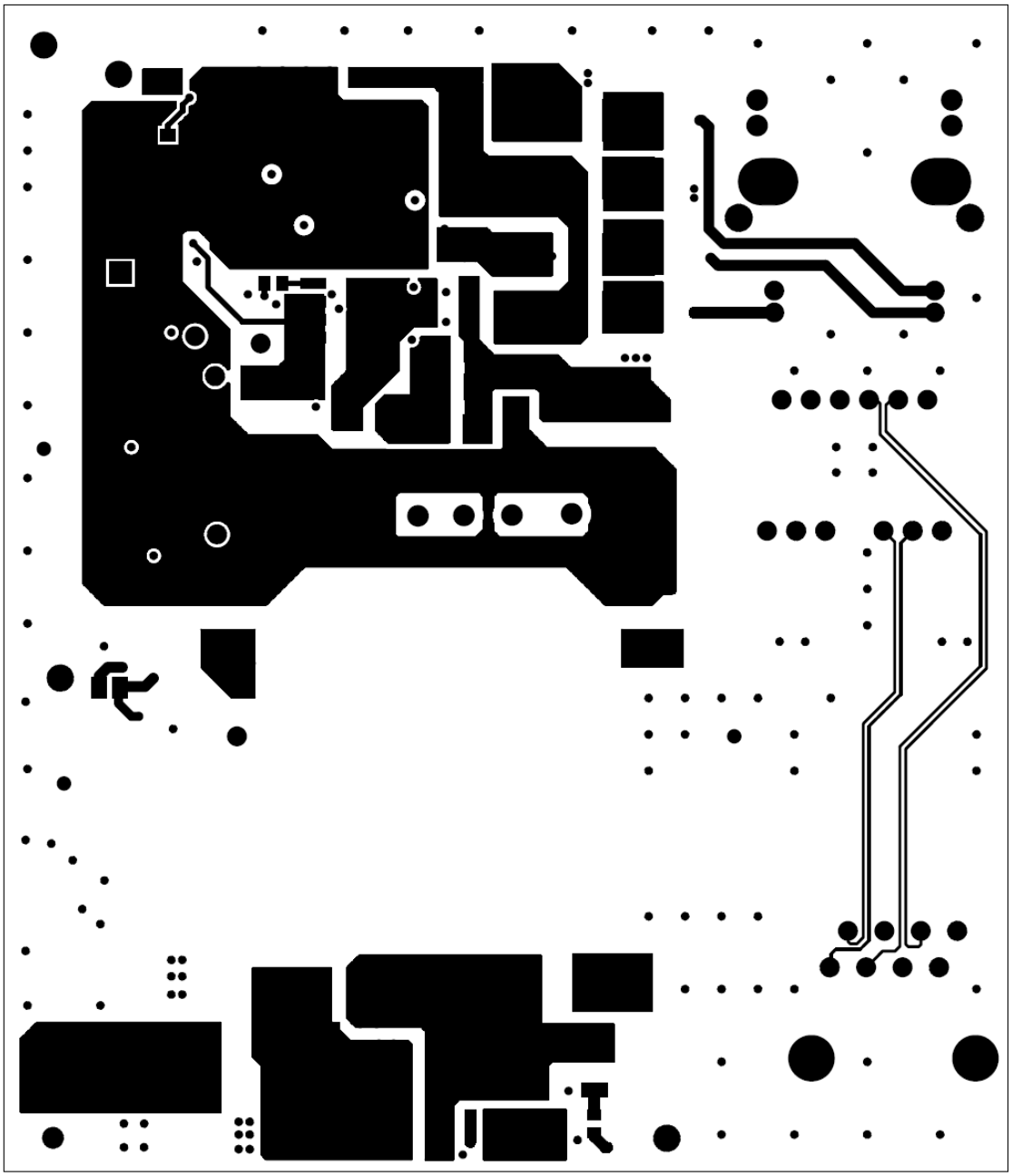
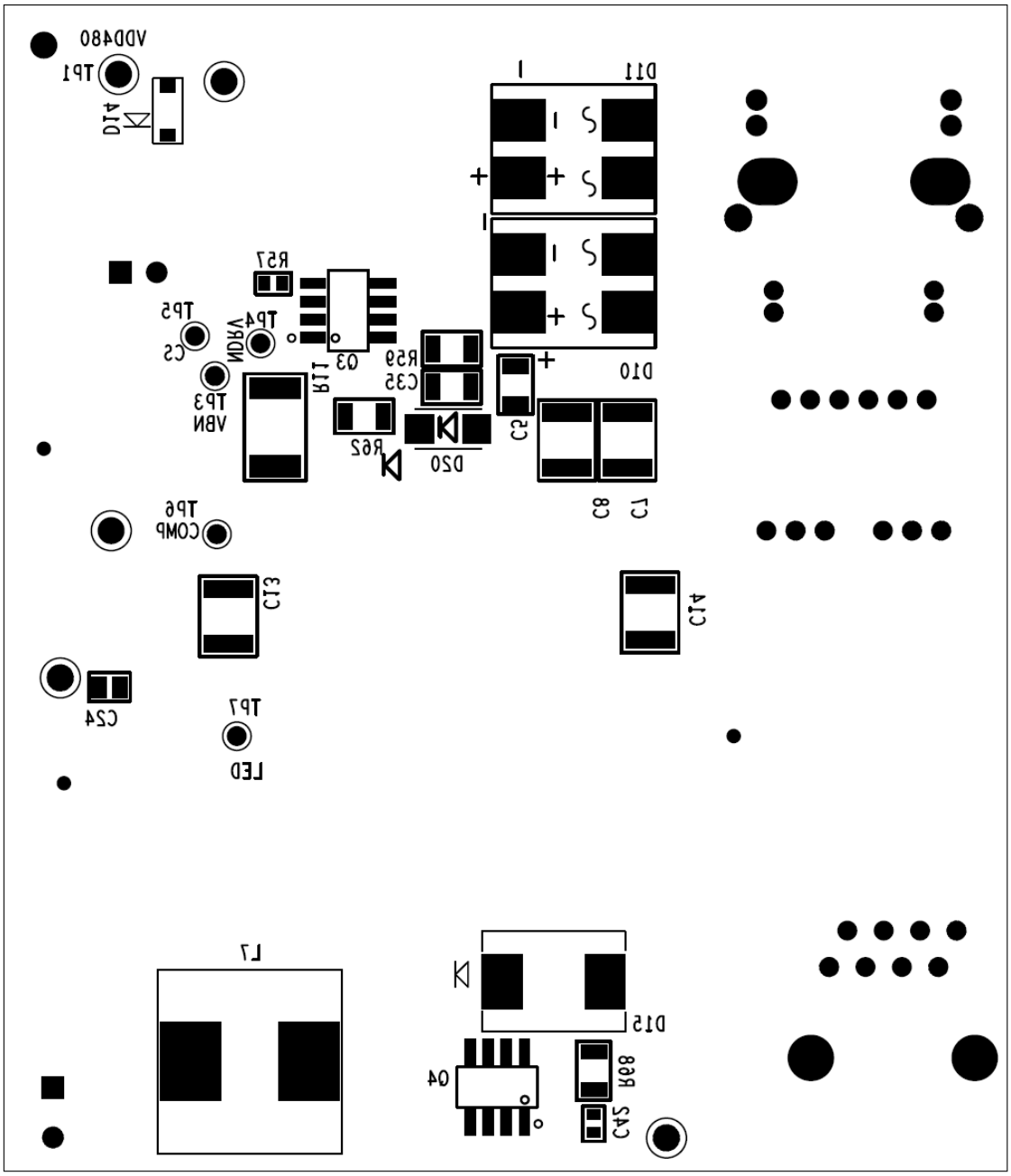


Figure 11 - Layout Example – Bottom Assembly



APPENDIX A - EXAMPLE SCHEMATICS

Figure 12 - Schematic of AS1138-EV-SYNC-FL5V30W (Line Interface and PD)

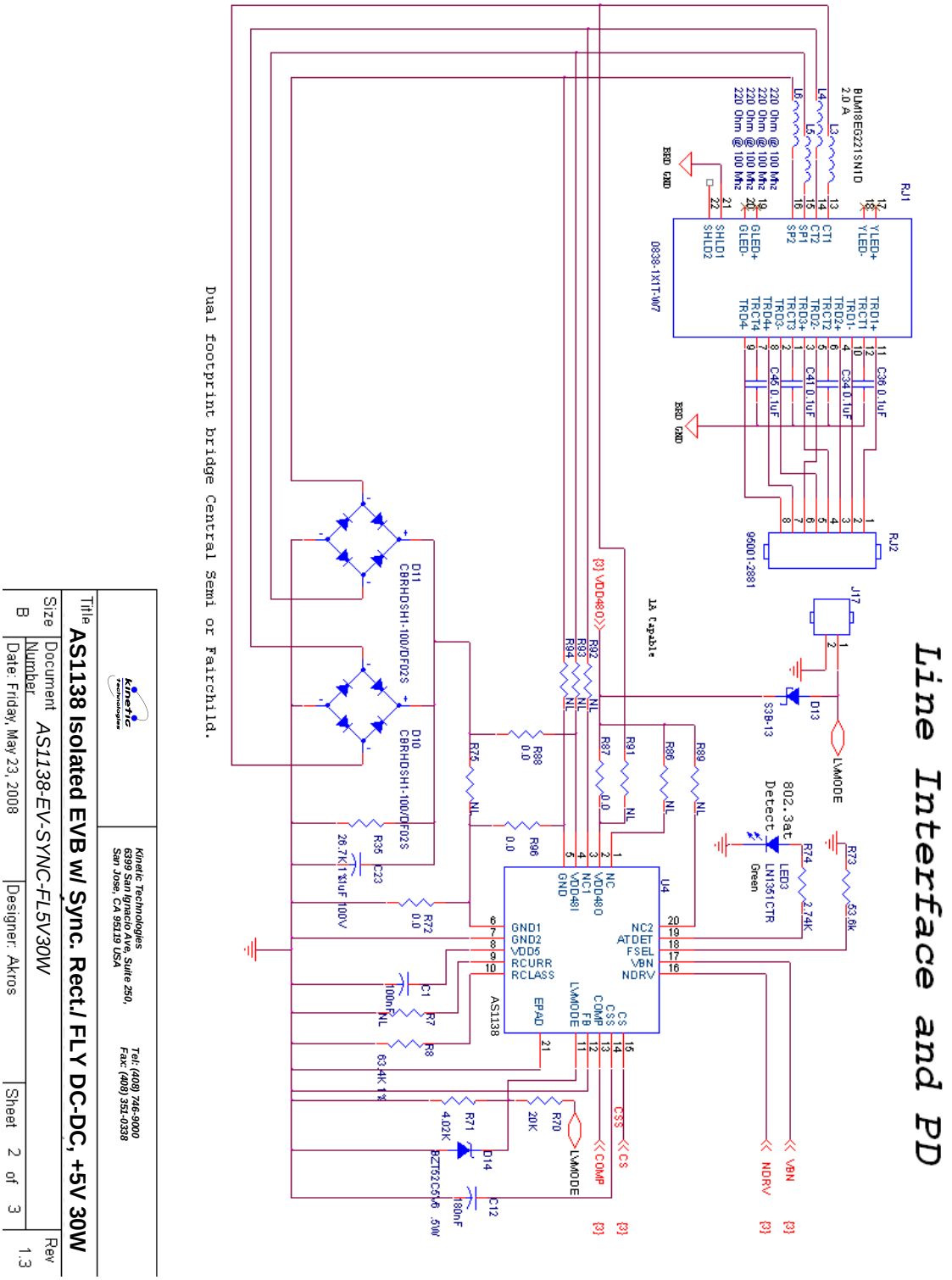
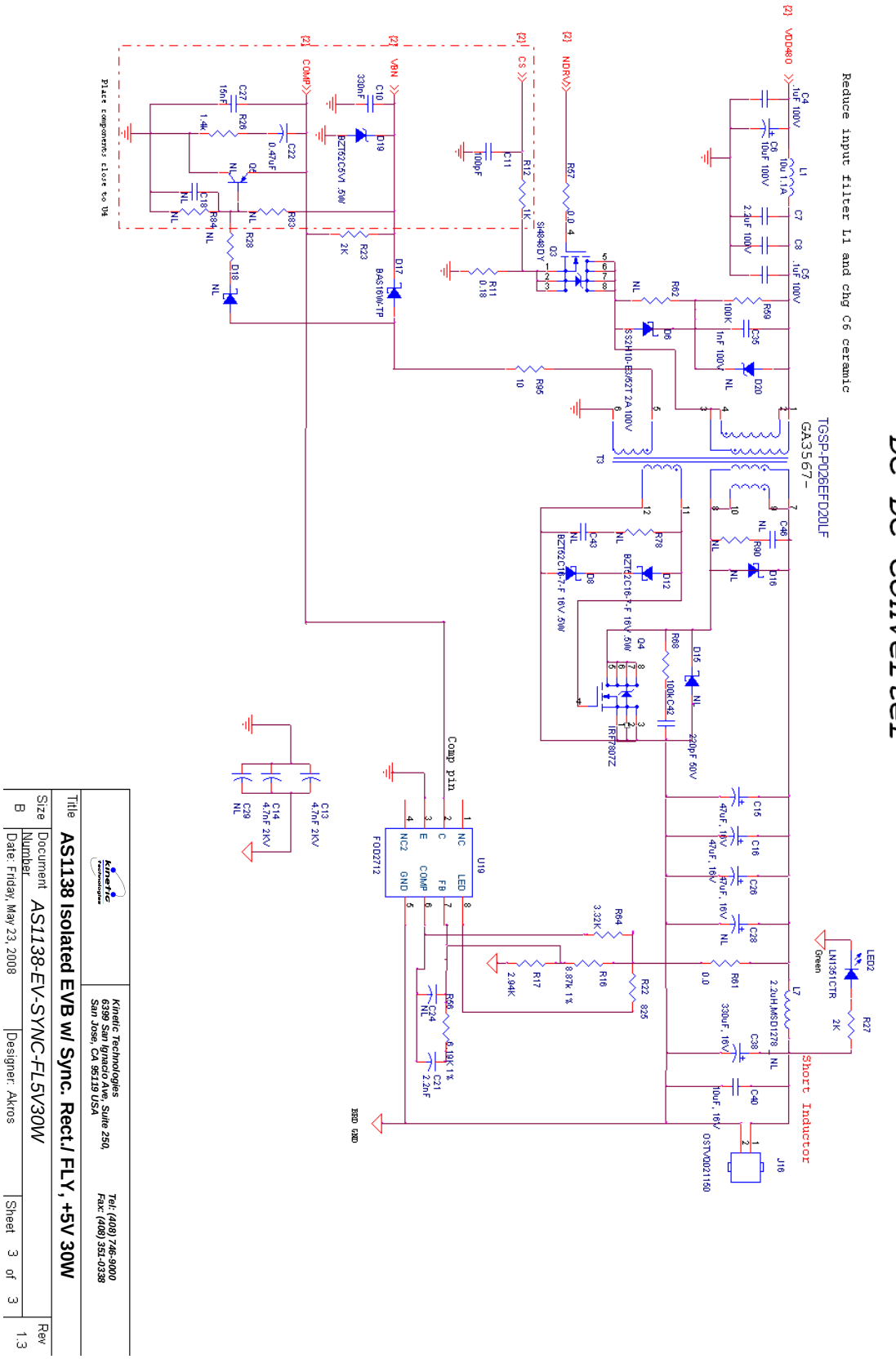


Figure 13 - Schematic of AS1138-EV-SYNC-FL5V30W (DC-DC Converter)



REFERENCE MATERIALS

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- Kinetic Technologies Application Note:
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  AS1138-EV-FL3.3-30W

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